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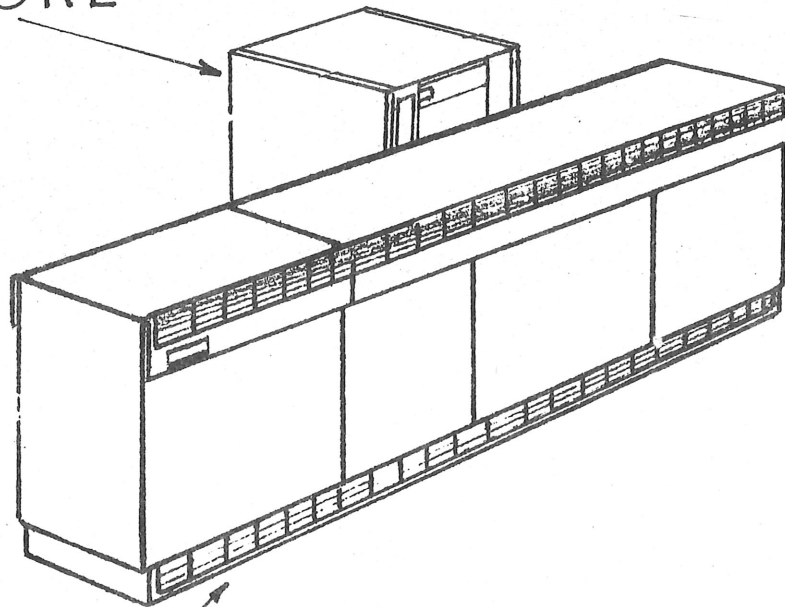
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\* To be supplied



# 1903 T Processor

STORE



CPU



1.0 INTRODUCTION

- 1.0.1 The 1903T is a medium-power, general-purpose processor, designed to process both commercial and scientific applications. Systems may be configured from the components listed in 2.1 and 2.2 below and the peripherals listed in Appendix A under the type of Executive used. All connected peripherals must be able to run simultaneously and appropriate I/O Channels must be provided for them.
- 1.0.2 Any 1903T system may be enhanced to a 1904S system in the field.

1.1 Summary of Characteristics

Order Code Level	C
Main Store Cycle Time	800 Nanoseconds
POWU II	4.0 Milliseconds
GAMM Mix (with H/W Option F1160/00)	15.0 Microseconds
Total I/O throughput: with High Speed Channel	2.5 Mch/second
without High Speed Channel	1.9 Mch/second
Main Store Size (MOS Store)	64K words to 192K words

2.0 TYPE NUMBERS & CONSTITUENT ITEMS

2.1 Standard Components

Type Number	Description
2043/00	Central Processor comprising the following: Central Processor Unit (CPU) including: (a) 8 Hardware Accumulators (b) Real Time Clock (c) Mill Timer (d) Slow Hesitation Control (SHC) with 6 Slow Channels Peripheral Autonomous Control (PAC) with 4 Fast Channels. DC Power Supply Units Console Typewriter Desk with Console Typewriter and operator's controls for loading and running the system. Extension Console Typewriter Desk with Console Typewriter and operator's controls permitting isolation of faulty store modules and switching control between the two Console Typewriters.
2043/03	64K words of Main Store )
2043/05	96K words of Main Store )
2043/06	128K words of Main Store )
2043/08	192K words of Main Store )
	(includes a Store Extension Unit)

## 2.2 Optional Hardware Features

The following items may be supplied either as part of the original order or as field fitments:

Type Number	Description
F1160/00	Floating Point Unit
F1161/00	Fast Peripheral Channel (maximum 8)
F1162/00	High Speed Channel (maximum 1)
F1163/00	Group of 6 Slow Channels (maximum 2)
F1165/00	Paging Feature
F1900/00	Main Store Switching Feature (permits store switching between two adjacent 1903T systems). Comprises additional store cables and SEU's as required; see 5.3.2 for ordering procedure.

## 2.3 Conversions

Type Number	Description
C1284/00*	Conversion of 2043/00 to 2046/00 (1903T to 1904S)
C1285/00	Conversion of 2043/03 to 2043/05
C1286/00	Conversion of 2043/05 to 2043/06
C1287/00	Conversion of 2043/06 to 2043/08

\*Includes upgrading of the Main Store performance

## 2.4 Basic Accessories

The items listed below are provided automatically, free of charge, with each 1903T Central Processor.

Description	Qty.
Console Chair	1
Console Typewriter Stationery (8½" x 200" roll, 2-part)	) 1 each per 2 ) Console
Ribbons	2 ) Typewriter

Additional supplies may be obtained from Dataset and are chargeable to the customer.

## 3.0 CONNECTIVITY

3.0.1 There are three aspects of connectivity relating to the attachment of 1900 Series peripherals to 1903T that must be satisfied:

- a) All connected peripherals must be supported by the Executive(s) to be used with the system.
- b) The correct type of I/O Channel must be provided for the connection of each peripheral.
- c) The total peripheral configuration must be able to run with simultaneity.

To satisfy requirement a) it is necessary to determine the

type of Executive(s) to be used by reference to 4.0 below, then to refer to the Approved Central Processor/Peripheral Connections table for that Executive(s), given in Appendix A to determine whether any given peripheral(s) is supported by that Executive(s). To satisfy requirements b) and c) use the information given in 3.1 below in conjunction with the 1903T, 1904A, 1904S Peripheral Simultaneity Rules given in Appendix B.

### 3.1 I/O Channels & Peripheral Simultaneity

- 3.1.1 The 1903T, 1904A, 1904S Peripheral Simultaneity Rules determine the types of I/O channels that can be used with different types of peripherals on these processors and give the loading figures (IMTAC Value or  $\alpha$  - Factor) applicable to each peripheral. The maximum number of I/O channels of each type available, the maximum number of data buffers in PAC and the maximum peripheral loading values permitted on 1903T are as follows:

Maximum number of High Speed Channels	1 (optional)
Maximum number of Fast Channels	12 (basic 4 + 8 optional)
Maximum number of Slow Channels	18 (basic 6 + 2 groups of 6 optional)
Maximum number of Data Buffers on PAC	5 (supplied as required)
Maximum IMTAC value allowed on PAC	625
Maximum IMTAC value per Data Buffer	95
Maximum IMTAC value per Fast Channels:	
(i) If no High Speed Channel on PAC	475
(ii) If High Speed Channel on PAC	625 - IMTAC value of the peripheral on the High Speed Channel or 475 whichever is less.

Maximum  $\alpha$  - Factor allowed on SHC is given by:

$$650 - 0.25I$$

(where I = the total IMTAC-value on PAC, see Appendix B, 3.0.6)

## 4.0 EXECUTIVE

- 4.0.1 The following Executives may be used with a 1903T:

Unpaged system or paging switched OFF	Paged system with paging switched ON
<u>E6RM</u>	<u>EWG4 (with GEORGE 4)</u>
EWG3 (with GEORGE 3)	

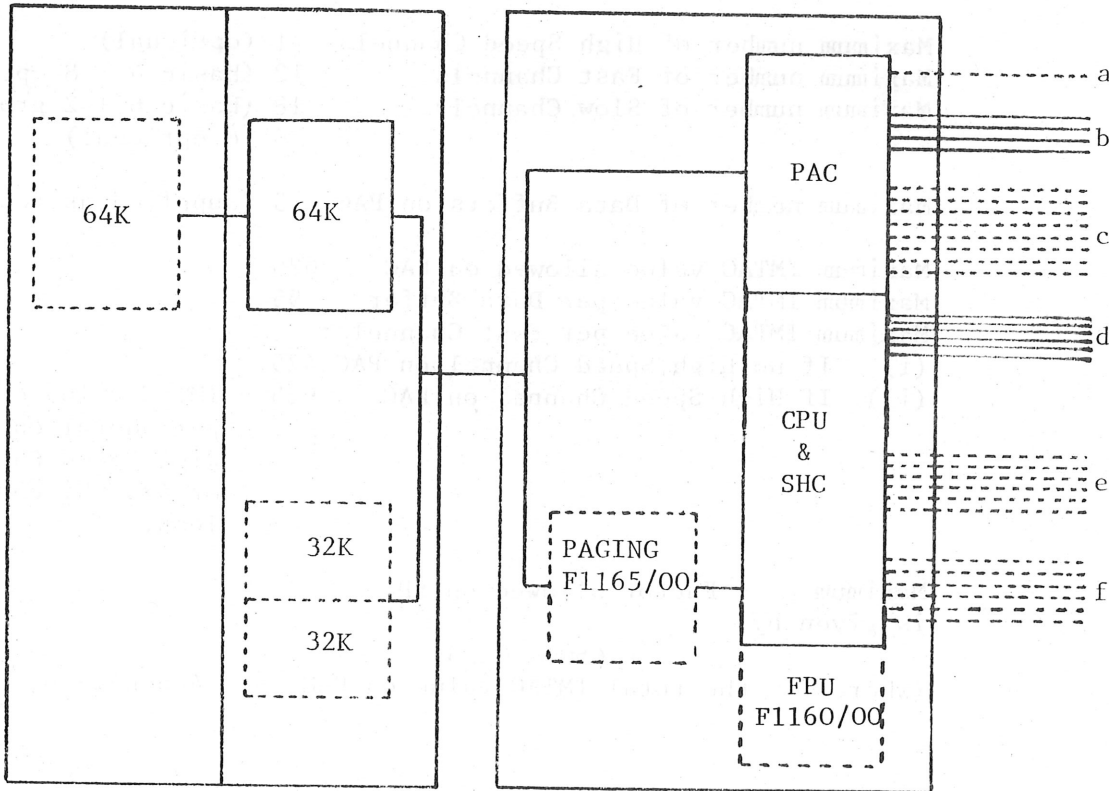
For further details of Executive, including compile-time options, store occupancy and peripheral requirements see Section 2.

5.0 HARDWARE GENERAL DESCRIPTION

5.1 System Description

5.1.1 The CPU, PAC and all optional features are implemented in TTL technology and are housed in a 3-bay cabinet structure which also houses the processor DC power supplies. The main store is implemented in TTL technology and Metal Oxide Semiconductor (MOS) storage elements and is housed in separate store cabinets, each capable of holding up to 128K words. The processor/store interface is effectively 25 bits wide, 24 bits + parity, and access can only be made to one store location at a time.

5.1.2 The logical structure of the system is shown in Figure 1 below:



- a = High Speed Channel (F1162/00)
- b = 4 Basic Fast Channels
- c = Additional Fast Channels each (F1161/00)
- d = 6 Basic Slow Channels
- e = 1st Enhancement Block of 6 Slow Channels (F1163/00)
- f = 2nd Enhancement Block of 6 Slow Channels (F1163/00)

Figure 1 Logical Structure of 1903T

## 5.2 Central Processor

5.2.1 The 1903T Central Processor is store image compatible with 1904A, 1904S, 1904E/F and 1906 in respect of data and instruction formats and implements the 1900 Series order code to C2 level. For list of instructions and timings see 8.0 Performance. Hardware Accumulators, Real Time Clock, Mill Timer, the ability to generate an interrupt on detection of a main store parity failure and main store isolation switches are all provided as standard.

### 5.2.2 REAL TIME CLOCK

The Real Time Clock enables Executive to output the date and time on all console messages, is used by GEORGE for scheduling and logging purposes and enables the GIVE instruction to be used to obtain the date and time as required by programmers.

Resolution = 200 Milliseconds

### 5.2.3 MILL TIMER

The Mill Timer (also called Program Timer) counts machine beats or clock pulses into a hardware register while the processor is in Object Program Mode. It does not count any beats due to processing within the Floating Point Unit although it counts those beats due to any fixed point instruction which is proceeding simultaneously. It does not count during extra codes or hesitations. When the register is almost full the contents are added to the clock count for that particular program held by Executive. The Executive message CLOCKED NN refers to millions of clock pulses and not seconds. In order to obtain an estimate in seconds for the 1903T the CLOCKED NN figure should be multiplied by 0.8.

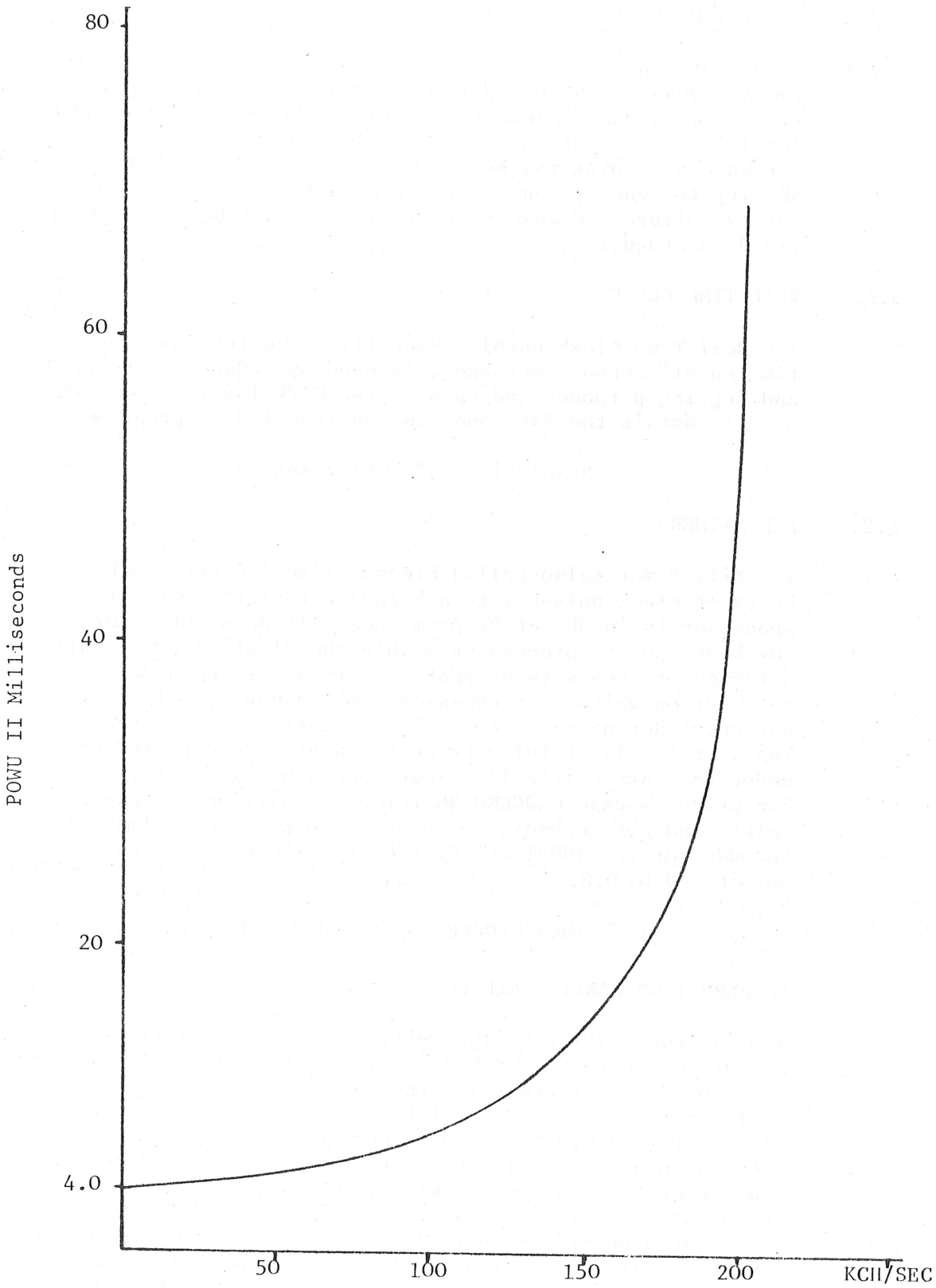
Thus CLOCKED NN x 0.8  $\approx$  PP seconds.

### 5.2.4 INTERRUPT ON PARITY FAILURE

A main store parity failure will cause an interrupt to Executive. Either GEORGE 3/4 or Executive will take action to suspend the program(s) using the store block affected and will generate a message to inform the operator. If the store block affected by the failure contains Executive or GEORGE then the processor will be HALTED. Two rotary switches mounted on the Console Typewriter Desk allow the operator to isolate faulty store blocks. Any one 32K word block may be isolated on stores up to 128K words. Two 32K word blocks may be isolated on stores greater than 128K words. In all cases the non-isolated store remains consecutively addressed.

### 5.2.5 PERIPHERAL HANDLING

Peripheral data transfers are handled by either the SHC or the PAC depending on the peripheral type (see Appendix B for details) and information concerning:



SHC Data Transfer Rate Kch/second

Figure 2 1903T Performance Degradation Due To SHC Activity

- (a) the number of outstanding units of transfer,
- (b) the absolute address of the next unit and
- (c) the style of transfer

are held in control words, which are read and updated once for each unit of data written to or read from main store. The four characters of a burst from a burst-mode peripheral are assembled into one word before being presented to main store.

5.2.6 SLOW HESITATION CONTROL

The SHC is an integral part of the CPU and the CPU mill is used to update the control words which are held in main store. The processor's B-register is used to assemble 4-characters serially into one word during a burst-mode transfer. For these reasons a data transfer via SHC and instruction processing cannot go on simultaneously and a peripheral request for data transfer must wait until the processor's mill and registers are in a condition to deal with the request. After such a delay the processing of instructions will hesitate for the duration of the transfer. The maximum CPU delay and SHC hesitation times, assuming no interference from PAC which has priority for main store access, are given below:

Type of Hesitation	Nominal Time in microseconds	
	Input	Output
Single Character Single Channel	) Individual times to be supplied. Meanwhile assume time spent in each SHC hesitation routine = 18.8 microseconds.	
Four Character Single Channel		
Single Character Multi Channel		
Four Character Multi Channel		
Control Word Recharge		
Scatter read-gather write*		
Maximum CPU delay		

\*Only when the paging feature is used and when a page boundary is crossed.

The effect of data transfers via the SHC on processor performance is indicated in Figure 2.

5.2.7 PERIPHERAL AUTONOMOUS CONTROL

The PAC is an autonomous unit having direct access to main store, a mill to update the control words, control word buffers and data buffers. Its logical structure is shown in Figure 4 below. The control word buffers and data buffers are supplied as required; one pair of control word buffers per channel connected, High Speed data buffers and up to 5 Fast data buffers depending on the number and type of peripherals connected. Since PAC has priority for store access, the processor will be forced to hesitate when a clash occurs, consequently instruction processing may be held up or SHC hesitations may be interrupted. However, since many operations in the central processor do not involve the store, the average delay experienced by the processor will be significantly

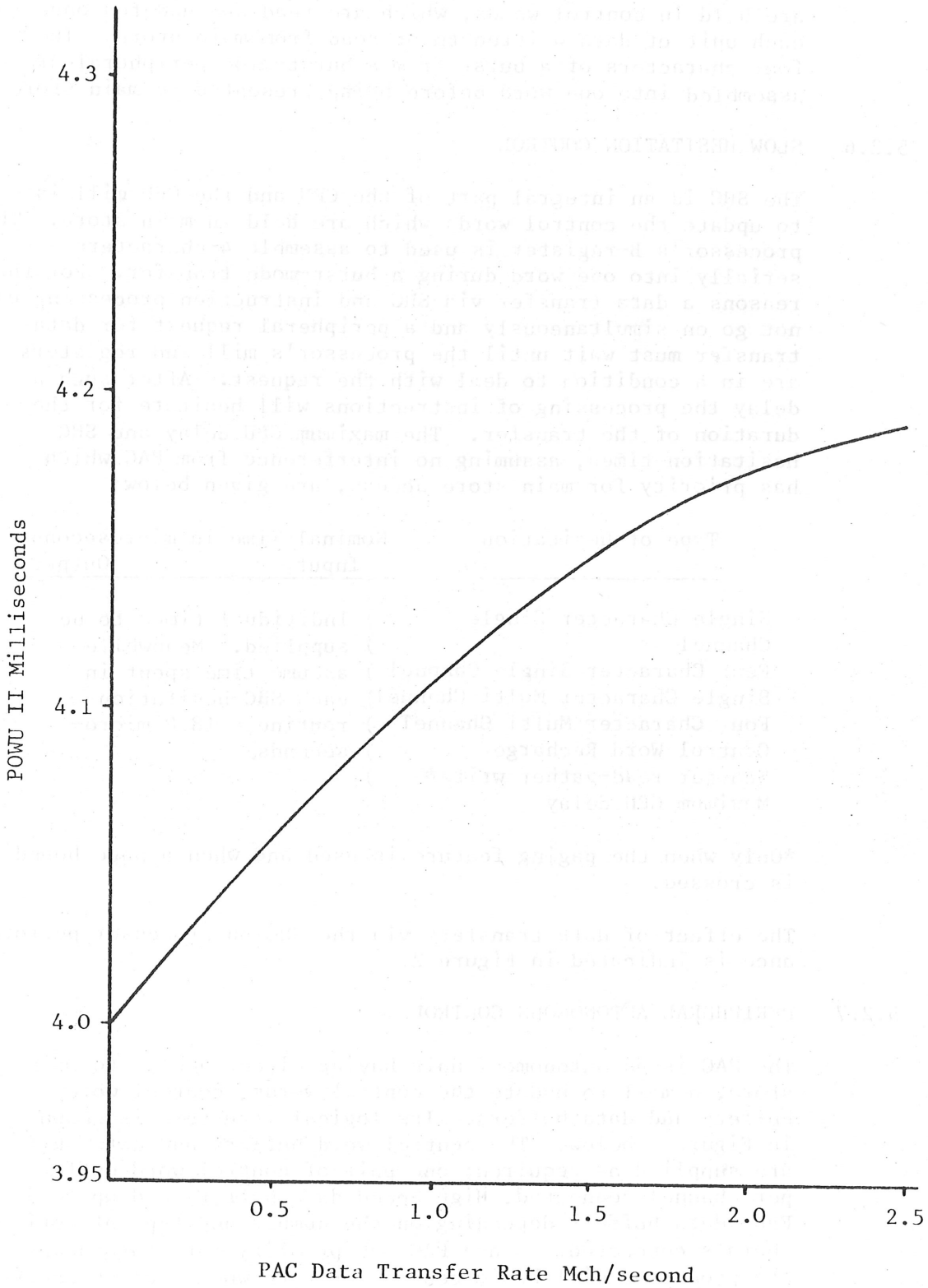


Figure 3 1903T Performance Degradation Due to PAC Activity

less than the maximum and is taken into account in calculating the degradation in processor performance due to PAC activity illustrated in Figure 3. The simultaneity rules take account of the effect of PAC on SHC timings.

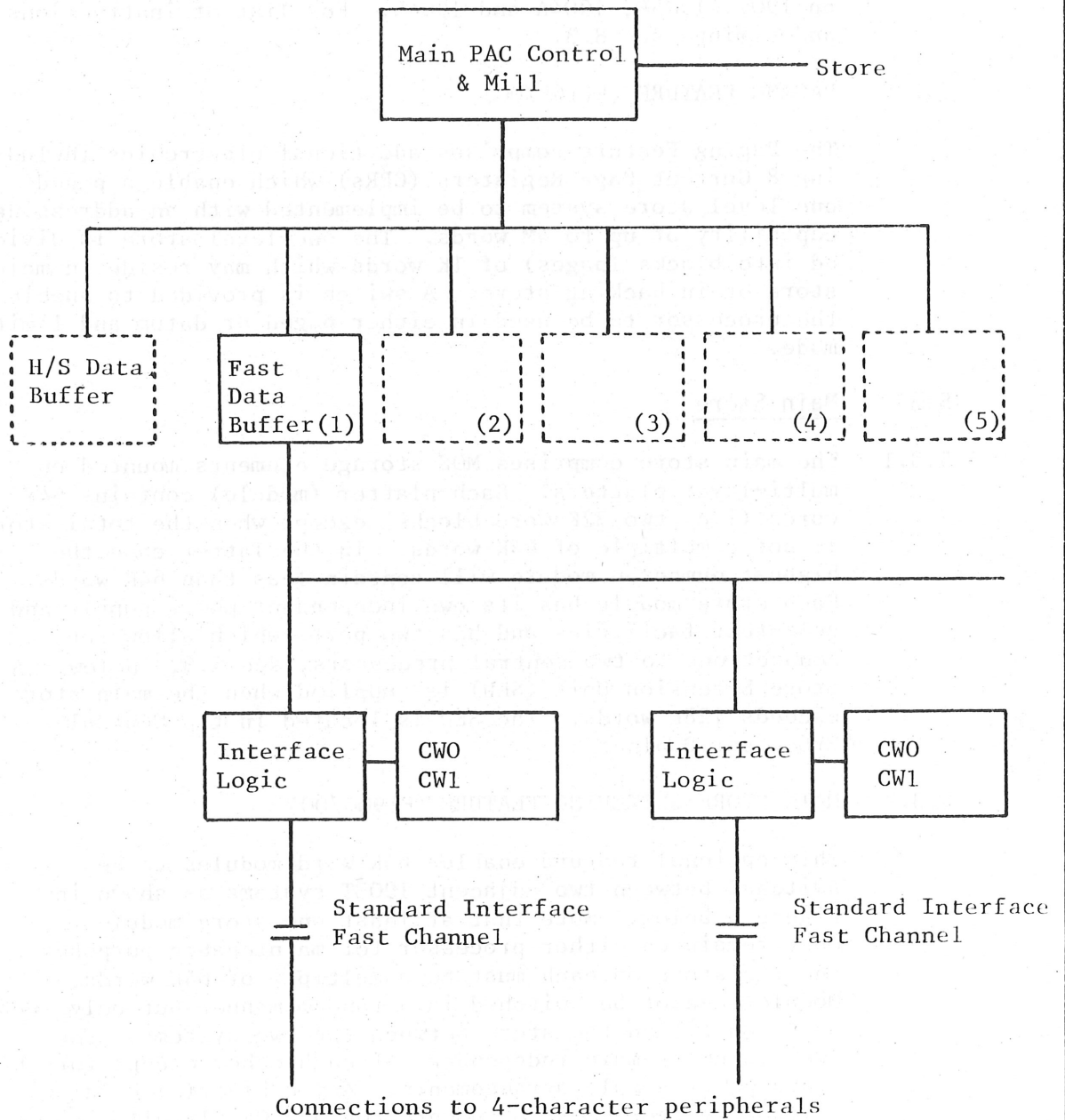


Figure 4 Logical Structure of 1903T PAC

### 5.2.8 FLOATING POINT UNIT (F1160/00)

The Floating Point Unit comprises additional electronics including a hardware floating point accumulator. It operates autonomously with the CPU during the execution phase of floating point instructions and provides results identical to those obtained with the Floating Point Units on 1907, 1905F, 1904A and 1904S. For list of instructions and timings see 8.3.

### 5.2.9 PAGING FEATURE (F1165/00)

The Paging Feature comprises additional electronics including 8 Current Page Registers (CPRs) which enable a paged one-level store system to be implemented with an addressing capability of up to 4M words. The one-level store is divided into blocks (pages) of 1K words which may reside in main store or in backing store. A switch is provided to enable the processor to be used in either paged or datum and limit mode.

## 5.3 Main Store

5.3.1 The main store comprises MOS storage elements mounted on multi-layer platters. Each platter (module) contains 64K words (i.e. two 32K word blocks) except when the total store is not a multiple of 64K words. In the latter case the highest numbered module will contain less than 64K words. Each store module has its own independent power supply and self-test facilities and has two ports which allow for connections to two central processors, see 5.3.2 below. A Store Extension Unit (SEU) is supplied when the main store exceeds 128K words. The SEU is located in the Central Processor Cabinet.

### 5.3.2 MAIN STORE SWITCHING FEATURE (F1900/00)

This optional feature enables 64K word modules to be switched between two adjacent 1903T systems as shown in Figure 5 below. Note that at least one store module must remain on either processor for maintenance purposes and the store on each must be a multiple of 64K words. Modules cannot be switched in a random manner but only such as to partition the store between the two systems. The two systems remain independent of each other except for the store power supply arrangements. Any cabinet(s) holding switchable store must be powered ON and OFF locally at that cabinet(s). One cabinet will be associated with each processor and an over-temperature condition occurring in a store cabinet will power OFF that cabinet and cause an interrupt only to the processor associated with that cabinet. The other processor will not receive an interrupt even though part of the store housed in that cabinet is switched to it.

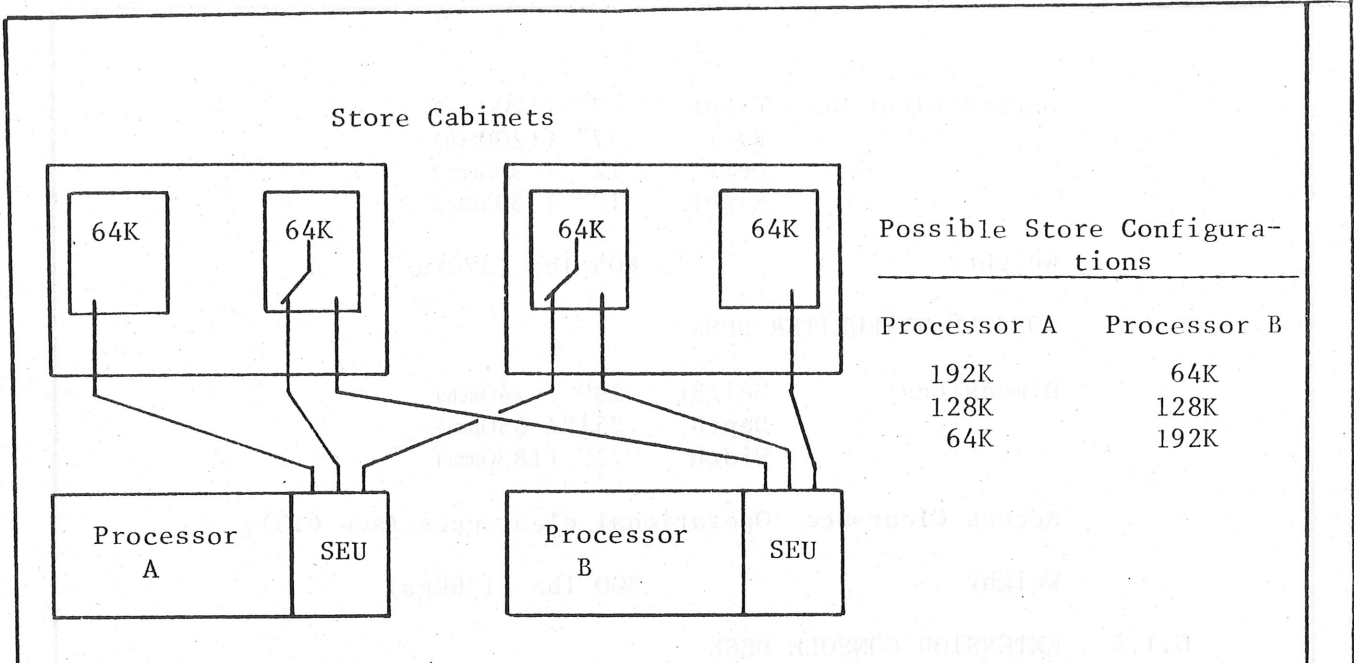


Figure 5 Store Switching Between Two Adjacent 1903T Processors

Note: Ordering Procedure

F1900/00 may be ordered against either one of the two systems. Main store must be ordered on both systems, i.e. it cannot all be specified against one system only. When F1900 is ordered, the number of store modules to be switched and the other system number must be stated so that the correct number of cables and SEUs can be supplied. The store specified on either system must not exceed 128K words.

6.0 PHYSICAL CHARACTERISTICS

6.1 Dimensions & Weight

6.1.1 CENTRAL PROCESSOR

Dimensions	Height	55" (1400mm)
	Depth	28½" (720mm)
	Length	140" (3556mm)
Access Clearance	Front	54" (1370mm)
	Rear	54" (1370mm)
	Left	-
	Right	36" (910mm)
Weight		1500 lbs (681Kgs).

6.1.2 MAIN STORE CABINET

Dimensions	Height	67" (1700mm)
	Depth	29½" (749mm)
	Length	27" (689mm)

Access Clearance	Front	47" (1200mm)
	Rear	47" (1200mm)
	Left	12" (305mm)
	Right	12" (305mm)

Weight 605 lbs (270Kgs)

### 6.1.3 CONSOLE TYPEWRITER DESK

Dimensions	Height	29" (740mm)
	Depth	25½" (650mm)
	Width	72" (1830mm)

Access Clearance Operational clearances (see 6.5).

Weight 300 lbs. (136Kgs)

### 6.1.4 EXTENSION CONSOLE DESK

Dimensions	Height	29" (740mm)
	Depth	25½" (650mm)
	Width	36" (914mm)

Access Clearance Operational clearances (see 6.5).

Weight 200 lbs (91Kgs)

## 6.2 Mains Supply

A Motor Alternator is mandatory. This may be either 1986/02 (45KVA) or 1986/07 (65KVA) depending on the total system requirements.

In either case the mains supply required will be 3 phase 50Hz.

## 6.3 Power Requirements & Heat Dissipation

6.3.1 Power Required	Central Processor	4.1 KVA
	Main Store 64K	1.2 KVA
	96K	2.0 KVA
	128K	2.0 KVA
	192K	3.2 KVA
	Consoles	0.4 KVA

6.3.2 Heat dissipation	Central Processor	3.0 KW
	Main Store 64K	0.945 KW
	96K	1.6 KW
	128K	1.6 KW
	192K	2.545 KW
T/W Consoles	0.3 KW	

## 6.4 Environment

Temperature range	10°C - 35°C
Relative Humidity	20% - 80%
Air Cleanliness	Air filtering not required under normal office conditions

6.5 Site Layout

6.5.1 The possible relative positions of the Central Processor, Main Store and Console Typewriter Desk are determined by the physical space available, cable lengths, access clearance required and the operational requirements of the system as a whole. CED Environmental Engineering must be consulted regarding all site layouts and can advise on the best layout taking into account all the relative factors.

The details given below are for guidance only:

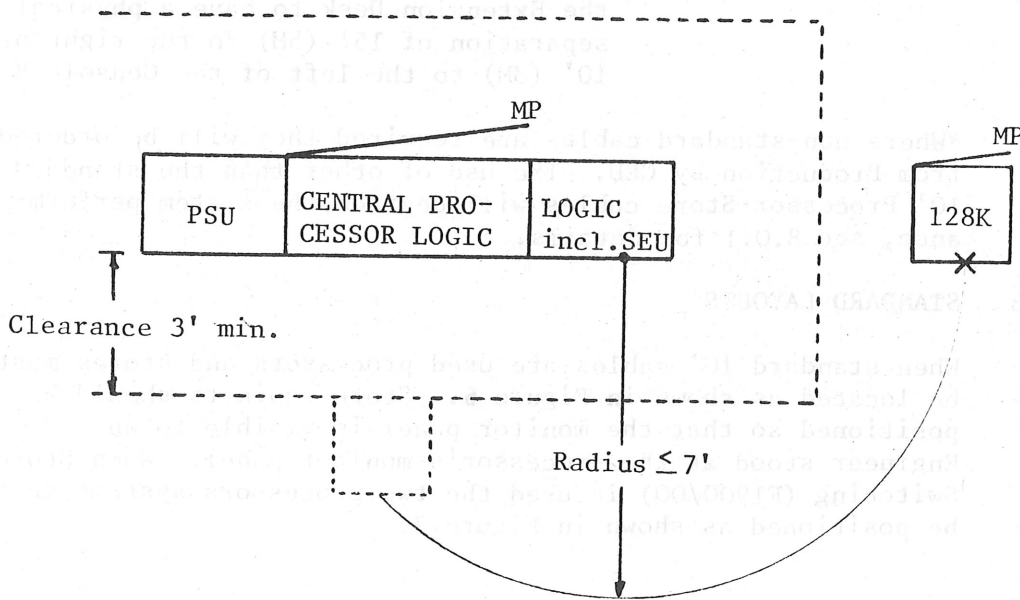
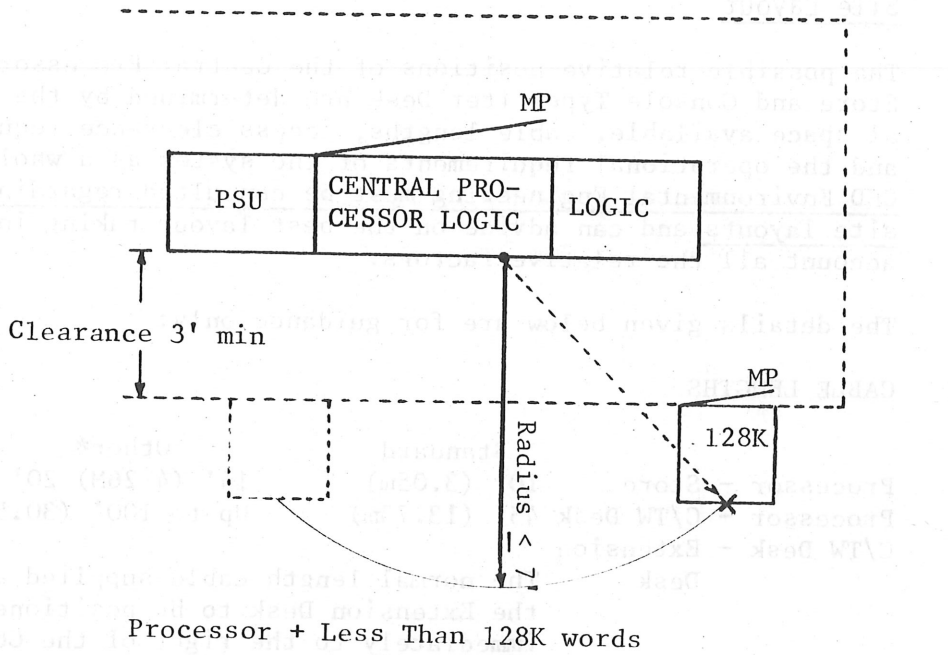
6.5.2 CABLE LENGTHS

	Standard	Other*
Processor - Store	10' (3.05m)	14' (4.26M) 20' (6.1M)
Processor - C/TW Desk	45' (13.73m)	Up to 100' (30.5M)
C/TW Desk - Extension Desk	The normal length cable supplied allows the Extension Desk to be positioned immediately to the right of the Console Desk. For a remote position, cables of length 20' (6.1M) are available allowing the Extension Desk to have a physical separation of 15' (5M) to the right or 10' (3M) to the left of the Console Desk.	

\*Where non-standard cables are required they will be ordered from Production by CED. The use of other than the standard 10' Processor-Store cables will degrade the system performance, see 8.0.1 for details.

6.5.3 STANDARD LAYOUTS

When standard 10' cables are used processors and stores must be located as shown in Figure 6. Store cabinets should be positioned so that the monitor panel is visible to an Engineer stood at the processor's monitor panel. When Store Switching (F1900/00) is used the two processors systems must be positioned as shown in Figure 7.



Processor + Greater Than 128K words

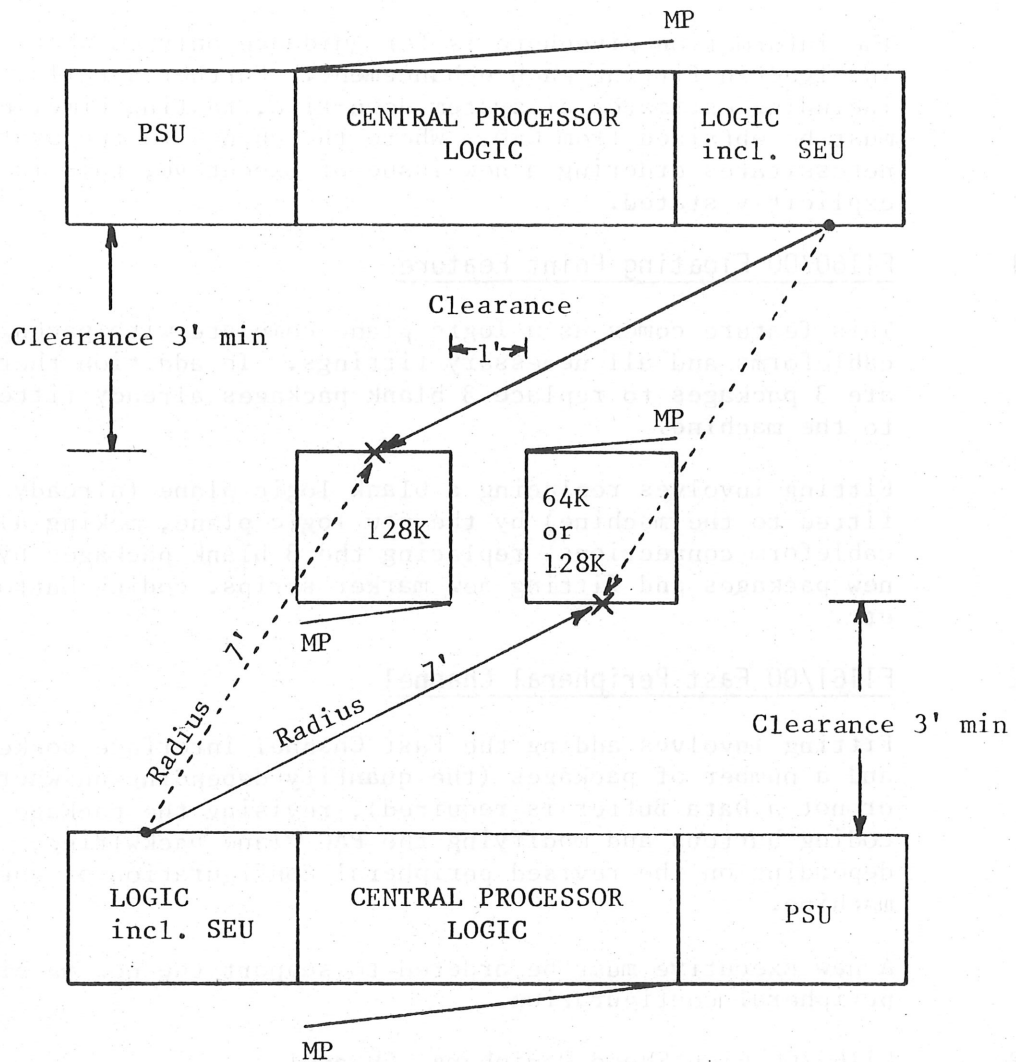
PSU = Processor Power Supply Units

• = Processor cable entry

X = Store cable entry

MP = Monitor Panel

Figure 6 1903T Processor/Store Standard Site Layouts



- PSU = Processor Power Supply Units
- = Processor cable entry
- X = Store cable entry
- MP = Monitor Panel

Figure 7 Standard 1903T Processor/Store Site Layout With Store Switching (F1900/00)

## 7.0 FIELD ENHANCEMENTS

The information given here is for guidance only on what is involved in fitting each enhancement. Further details, including estimates of system down-time, testing time, etc. must be obtained from CED. Where the change to the system necessitates ordering a new issue of Executive, this is explicitly stated.

### 7.1 F1160/00 Floating Point Feature

This feature comes as a logic plane complete with packages, cableforms and all necessary fittings. In addition there are 3 packages to replace 3 blank packages already fitted to the machine.

Fitting involves replacing a blank logic plane (already fitted to the machine) by the new logic plane, making all cableform connections, replacing the 3 blank packages by new packages and fitting new marker strips, coding buttons, etc.

### 7.2 F1161/00 Fast Peripheral Channel

Fitting involves adding the Fast Channel interface socket and a number of packages (the quantity depending on whether or not a Data Buffer is required), revising the package coding buttons and modifying the PAC Plane backwiring, depending on the revised peripheral configuration of the machine.

A new Executive must be ordered to support the new machine peripheral configuration.

### 7.3 F1162/00 High Speed Peripheral Channel

Fitting involves adding the High Speed Channel interface socket and making connections to the PAC Plane, replacing 7 packages, adding 2 additional packages and revising the package coding buttons.

A new Executive must be ordered to support the new machine peripheral configuration.

### 7.4 F1163/00 Group of 6 Slow Channels

Fitting involves adding the Slow Channel interface sockets and packages and connecting the channels to the corresponding channel positions on the Distribute Plane.

A new Executive must be ordered to support the new machine peripheral configuration.

### 7.5 F1165/00 Paging Feature

This feature comes as a logic plane assembly complete with packages, cableforms and all necessary fittings and an Engineers Control Panel and monitor panel.

Fitting involves replacing a blank logic plane (already fitted to the machine) by the new logic plane, fitting the Engineers Control Panel and monitor lamp panel, making the cableform connections and replacing blank packages in the Distributer Plane by new packages.

Order Executive EWG4 and GEORGE 4.

### 7.6 F1900/00 Main Store Switching Feature

Fitting involves connecting the store modules, to be switched, to the processor(s) via store interface cableforms and fitting SEU's if required.

### 7.7 C1284/00 Conversion of 2043/00 to 2046/00 (1903T to 1904S)

This conversion involves the replacement of 1 package in the CPU (2 if F1160/00 is fitted) and replacement of 1 Logic Macro on each store platter. Change the coding buttons where packages have been replaced and change the name inserts on the CPU, typewriter desk and store cabinets.

### 7.8 C1285/00 Conversion of 2043/03 to 2043/05

Fit 32K Store Macro Block to store platter and revise coding buttons.

### 7.9 C1286/00 Conversion of 2043/05 to 2043/06

Fit 32K Store Macro Block to store platter and revise coding buttons.

### 7.10 C1287/00 Conversion of 2043/06 to 2043/08

This conversion involves adding a 2nd Store Cabinet with 64K of store, linking the stores via cableforms and modifying the Distributer by changing and adding packages and revising the appropriate coding buttons.

## 8.0 PERFORMANCE

8.0.1 All performance figures quoted apply to 1903T systems without Store Extension Units (SEUs) and using standard 10' cables between the Central Processors and Main Stores. The figures quoted may be degraded due to store refresh, the addition of an SEU or the use of longer store cables by the percentages given below, except when explicitly stated otherwise.

- a) Less than 1% due to store refresh,
- b) Less than 4% if a SEU is fitted,
- c) Less than 1% due to the use of 14' store cables,
- d) Less than 2% due to the use of 20' store cables.

All tolerances where given, and degradation figures, where applicable, are additive.

## 8.1 Work Mixes

The timings will not be greater than the figures given below due to any machine tolerance but may be degraded by +1% -2% due to the method of measurement depending on the 50Hz mains frequency at the time of measurement. See also 8.0.1 above.

Post Office Work Unit II (POWU II)

Basic 1903T	4.0	milliseconds
Paging Switched OFF	4.3	"
Paging Switched ON	4.6	"

GAMM Mix (with F1160/00 fitted)

Non-paged machine	15.0	microseconds
Paging Switched OFF	16.0	"
Paging Switched ON	17.0	"

## 8.2 Fixed Point Instruction Times

8.2.1 The instruction times quoted below are subject to a tolerance of +10%. The timings may be further degraded as follows:

- a) By the figures given in Section 8.0.1 above.
- b) For paged machines by up to 2% due to the variable overheads of loading the current page registers.
- c) By an additional tolerance of +1% -2% due to the method of measurement depending on the mains frequency.

All times are applicable to 15 bit and 22 bit address modes of working.

FUNCTION	TIMING UNMODIFIED Microseconds	TIMING MODIFIED Microseconds
000	3.87	4.36
001	3.87	4.36
002	3.87	4.36
003	3.87	4.36
004	3.87	4.36
005	3.87	4.36
006	3.87	4.36
007	3.87	4.36
010	3.73	4.22
011	4.42	4.91
012	3.73	4.22
013	4.42	4.91
014	3.73	4.22
015	4.42	4.91
016	3.73	4.22
017	4.42	4.91
020	3.87	4.36
021	3.87	4.36
022	3.87	4.36
023	2.75	3.24
024	3.87	4.36
025	3.87	4.36
026	3.87	4.36
027	3.87	4.36
030	4.42	4.91
031	4.42	4.91
032	4.42	4.91
033	3.73	4.22
034	4.42	4.91
035	4.42	4.91
036	4.42	4.91
037	4.42	4.91
040	16.61 - 17.1	17.1 - 17.59
041	16.61 - 17.1	17.1 - 17.59
042	16.61 - 17.1	17.1 - 17.59
043	8.28	8.77
044	17.59 - 18.57	18.08 - 19.06
045	18.57 - 21.02	19.06 - 21.51
046	17.59 - 18.57	18.08 - 19.06
047	14.36	14.85
050	3.73	-
052	3.73	-
054	3.73	-
056	3.73	-

FUNCTION	TIMING UNMODIFIED Microseconds	TIMING MODIFIED Microseconds
060	3.73	-
062	3.73	-
064	3.73	-
066	3.73	-
070	4.22	-
072	4.22	-
074	3.24	-
076	3.24	-
100	3.73	-
101	3.73	-
102	3.73	-
103	3.73	-
104	3.73	-
Lo5	3.73	-
106	3.73	-
107	3.73	-
110	3.24 + 0.49N	-
112	3.24 + 0.49N	-
114	4.22 + 0.49N	-
116	9.75 + 4.69N	-
111	4.22 + 0.49N	--
113	4.22 + 0.49N	--
115	6.18 + 0.49N	--
117	4.85	5.34
120	3.73	-
121	3.73	-
122	3.73	-
123	3.24	-
124	7.16	-
125	3.73	-
126	8.26 + 1.67N	-
127	4.71 + 1.12N	-

N = Number of places shifted, moved or normalised.

### 8.3 Floating Point Instruction Times

8.3.1 The instruction times quoted below apply only to 1903T systems fitted with the F1160/00 Hardware Floating Point Unit. It is possible for both fixed point and floating point functions to be executed simultaneously. There are up to 4 phases applicable to floating point instructions and only phase 4 is capable of overlap.

8.3.2 In phase 1 the instruction is fetched from store by the central processor; in phase 2 the N address is modified; in phase 3 the central processor loads the operand into the floating point unit (or unloads the operand into

store), and in phase 4 the floating point unit executes the instruction. As soon as phases 1, 2 and 3 have been completed the central processor is free to continue with fixed point instructions or to execute phases 1, 2 and 3 of another floating point instruction (there is a buffer available in the floating point unit to queue a second floating point order). If phase 4 of the first instruction is still in progress and a third floating point instruction is encountered it will be executed to the end of phase 2 and the central processor will be held up until phase 4 of the first floating point instruction is completed. Since none of the 076, 136 or 137 instructions involve the floating point unit in any actual calculation, there can be no overlap for any instructions that follows them but if a 076, 136 or 137 instruction follows one of the other floating point orders, then overlap applies in the normal way.

8.3.3 The timings in microseconds for phases 1, 2 and 3 are as follows:

		Basic 1903T	Paging OFF	Paging ON
Phase 1	Fetch Instruction	2.80	2.94	3.01
Phase 2	Modification	0.50	0.50	0.50
Phase 3	Load Operand	1.85	2.13	2.51
Phase 3	Unload Operand	3.26	3.26	3.56

An SEU will not degrade the above times by more than:

- Phase 1 + 0.03 microseconds
- Phase 3 + 0.06 microseconds

For degradation due to store refresh or the use of longer than 10' standard cables see 8.0.1.

All above times are subject to a tolerance of + 10%.

8.3.4 Phase 4 timings are not subject to any degradation due to store refresh or the use of non-standard length store cables or paging. They are however subject to a machine tolerance of +5% plus an additional tolerance of +1% -2% due to mains frequency variation.

Timings in microseconds are as follows:

FUNCTION	130	131	132	133	134	135	136	137
MIN/U	-	2.8	4.2	4.2	14.0	31.5	-	-
MAX/U	-	35.7	13.3	13.3	14.7	35.0	-	-
MIN/N	3.5	-	5.6	5.6	15.4	32.2	-	-
MAX/N	36.4	-	39.2	39.2	66.5	59.5	1.4	1.4

MIN = Minimum calculation (no rounding, correction or alignment required)

MAX = Maximum calculation (rounding, correction and alignment required)

/U = Un-normalised operand (no normalising required)

/N = Normalised operand (normalising required)

## 8.4 I/O Performance

The figures given below are maximum data transfer rates and are given as general information only. They cannot be used as the basis of checking peripheral simultaneity because this depends on worst case maximum peripheral data transfer rates, crisis time considerations, the effect of PAC transfers on the SHC and other factors beyond the scope of this manual. The actual data transfer rate achieved on any system depends on the peripheral configuration, the connectivity to the system and the program(s).

Maximum I/O Throughput per system

- a) With a High Speed Channel used on PAC 2.5 Mch/second
- b) Without a High Speed Channel on PAC 1.9 Mch/second

Maximum data transfer rate of

- a) High Speed Channel 1.5 Mch/second
- b) Fast Channel (or PAC Data Buffer)  
(See Note 1) 380 Kch/second
- c) Slow Channel (See Note 2)
  - i) Burst Mode (4-Character) 80 Kch/second
  - ii) Single Character 30 Kch/second

NOTE 1: More than one Fast Channel may be connected to a PAC data buffer therefore the maximum data transfer rate of all Fast Channels sharing one data buffer is 380 Kch/second.

- 2: The maximum data transfer rate of a Slow Channel is the same as that for the SHC as a whole which is given by:

$\frac{10^6}{\text{Hesitation Time in microseconds}}$  (See 5.2.6).

However, because SHC activity heavily degrades the processor performance and is itself degraded by PAC activity it would not be sensible to allow fast peripherals to be connected via the SHC Slow Channels. The data transfer rates given for Slow Channels are not therefore the maximum imposed by the hardware but are a guide to the practical limits that are imposed. The Simultaneity Rules determine whether any given peripheral may be connected via a Slow Channel or not.

## 9.0 ORDER VETTING CHECKLIST

### NEW SYSTEM ORDERS

1. Check that the configuration includes all mandatory peripherals required for maintenance purposes and by Executive and/or Operating System. See 9.1 below and Section 2.
2. Check that the correct type of Motor Alternator has been specified. See 6.2.

### ENHANCEMENT ORDERS

3. Check that the correct system number has been quoted.

### ALL ORDERS

4. Check that all peripherals specified are supported by the Executive to be used on the system. See Appendix A.
5. Check peripheral simultaneity and that the correct quantity and types of I/O channels have been specified for the connection of all peripherals. See 3.1 and Appendix B.
6. Where peripheral switches have been specified check that a switching diagram has been included.
7. When peripherals have been retained from some earlier system or from other sources check that these are listed on the specification form.
8. Check that a diagram of all communications configurations is included on the Communications Specification form.
9. See appropriate peripheral ORDER VETTING CHECKLISTS for dependencies, features etc. applicable to the peripherals or peripheral sub-systems.

## 9.1 Mandatory Peripherals Required For Maintenance Purposes

It must be possible to have at least one suitable input device and one suitable output device connected to a system for maintenance purposes. Either these must be permanently connected to the processor or it must be possible to switch them to the processor by means of Standard Interface Switching Units. The only input devices suitable are either:

- a) An 80 column card reader - with or without Card Image  
or
- b) A paper tape reader capable of handling ISO 8 channel tape.

The only output devices suitable are either:

- a) A line printer with 96 or more print positions, buffered or unbuffered and connected to either PAC or to SHC.  
or
- b) A paper tape punch, provided there is on the customer's

premises an off-line printer which can accept the paper tape produced by this punch.