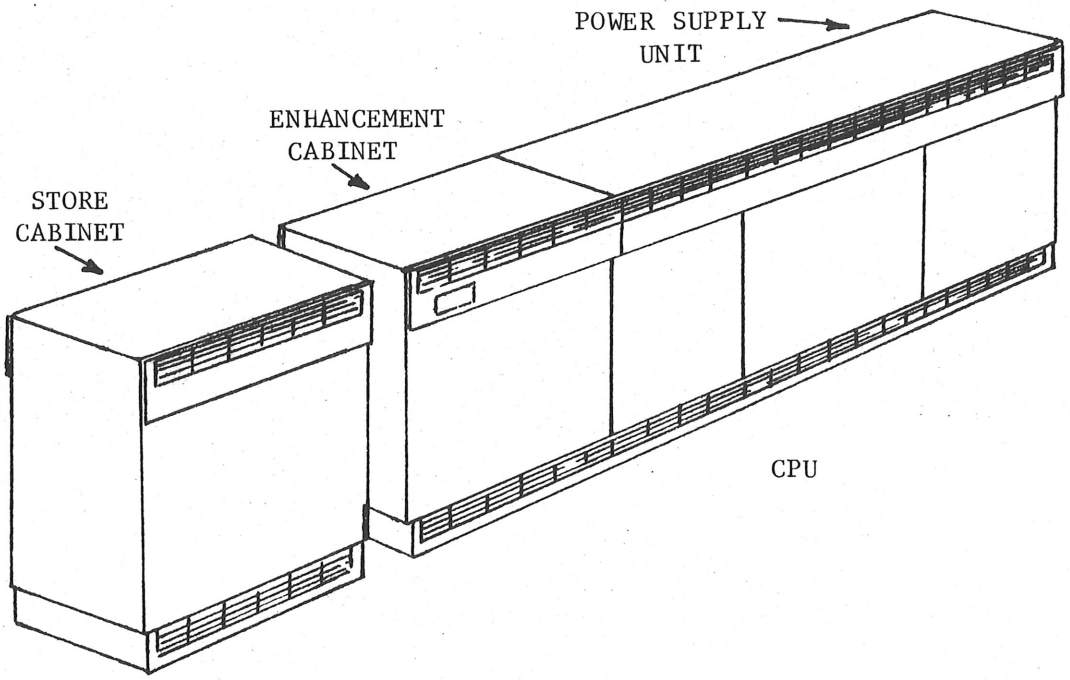
1904A Processor



1.0 INTRODUCTION

1.0.1 The 1904A is a medium-power, general-purpose processor, designed to process both commercial and scientific applications. Systems may be configured from the components listed in 2.1 and 2.2 below and the peripherals listed in Appendix A under the type of Executive used. All connected peripherals must be able to run simultaneously and appropriate I/O Channels must be provided for them.

1.0.2 1904A Central Processors from Machine No. 471 onwards may be enhanced to 1904S Central Processors. Earlier machines, up to and including Machine No. 470, may be enhanced to reduced facility 1904S Central Processors.

1.1 Summary of Characteristics

Order Code Level	C
Main Store Cycle Time	750 Nanoseconds
POWU II	3.0 Milliseconds
GAMM Mix (with H/W Option F1160/00)	11.0 Microseconds
Total I/O throughput: with High Speed Channel	3.0 Mch/second
without High Speed Channel	2.2 Mch/second
Main Store Size (Core Store)	32K words to 256K words

2.0 TYPE NUMBERS & CONSTITUENT ITEMS

2.1 Standard Components

Type Number	Description
2044/00	Central Processor comprising the following: Central Processor Unit (CPU) including (a) 8 Hardware Accumulators (b) Real Time Clock (c) Mill Timer (d) Slow Hesitation Control (SHC) with 6 Slow Channels Peripheral Autonomous Control (PAC) with 4 Fast Channels. DC Power Supply Units Console Typewriter Desk with Console Typewriter and operator's controls for loading and running the system. Extension Console Typewriter Desk with Console Typewriter and operator's controls permitting switching control between the two Console Typewriters.
2044/01	32K words 750 nsec Core Store)
2044/02	48K words 750 nsec Core Store)
2044/03	64K words 750 nsec Core Store)
2044/05	96K words 750 nsec Core Store) Select appropriate
2044/06	128K words 750 nsec Core Store) size
2044/08*	192K words 750 nsec Core Store)
2044/09*	256K words 750 nsec Core Store)

*Includes a Store Extension Unit

2.2 Optional Hardware Features

The following items may be supplied either as part of the original order or as field fitments:

Type Number	Description
F1160/00	Floating Point Unit
F1161/00	Fast Peripheral Channel (maximum 8)
F1162/00	High Speed Channel (maximum 1)
F1163/00	Group of 6 Slow Channels (maximum 2)
F1165/00	Paging Feature

2.3 Conversions

Type Number	Description
C1050/00	Conversion of 2044/01 to 2044/03
C1051/00	" " 2044/03 " 2044/05
C1052/00	" " 2044/05 " 2044/06
C1053/00	" " 2044/06 " 2044/08
C1054/00	" " 2044/08 " 2044/09
C1115/00	" " 2044/01 " 2044/02
C1116/00	" " 2044/02 " 2044/03
C1176/01	" " 2044/00 MARK 1 to 2046/00 MARK 1
C1176/02	" " 2044/00 MARK 2 to 2046/00 MARK 2 (See 5.2.1)

2.4 Basic Accessories

The items listed below are provided automatically, free of charge, with each 1904A Central Processor.

Description	Qty.	
Console Chair	1	
Console Typewriter Stationery ($8\frac{1}{2}$" x 200" roll, 2-part)	2	1 each per Console
Ribbons	2	1 each per Typewriter

Additional supplies may be obtained from Dataset and are chargeable to the customer.

3.0 CONNECTIVITY

3.0.1 There are three aspects of connectivity relating to the attachment of 1900 Series peripherals to 1904A that must be satisfied:

a) All connected peripherals must be supported by the Executive(s) to be used with the system.
b) The correct type of I/O Channel must be provided for the connection of each peripheral.
c) The total peripheral configuration must be able to run with simultaneity.

To satisfy requirement a) it is necessary to determine the type of Executive(s) to be used by reference to 4.0 below,

then to refer to the Approved Central Processor/Peripheral Connections table for that Executive(s), given in Appendix A, to determine whether any given peripheral(s) is supported by that Executive(s). To satisfy requirements b) and c) use the information given in 3.1 below in conjunction with the 1903T, 1904A, 1904S Peripheral Simultaneity Rules given in Appendix B.

3.1 I/O Channels & Peripheral Simultaneity

3.1.1 The 1903T, 1904A, 1904S Peripheral Simultaneity Rules determine the types of I/O channels that can be used with different types of peripherals on these processors and give the loading figures (IMTAC Value or α - Factor) applicable to each peripheral. The maximum number of I/O channels of each type available, the maximum number of data buffers in PAC and the maximum peripheral loading values permitted on 1904A are as follows:

Maximum number of High Speed Channels	1	(optional)
Maximum number of Fast Channels	12	(basic 4 + 8 optional)
Maximum number of Slow Channels	18	(basic 6 + 2 groups of 6 optional)
Maximum number of Data Buffers on PAC	6	(supplied as required)
Maximum IMTAC value allowed on PAC	750	
Maximum IMTAC value per Data Buffer	95	
Maximum IMTAC value per Fast Channels:		
(i) If no High Speed Channel on PAC	550	
(ii) If High Speed Channel on PAC	750	- IMTAC value of the peripheral on the High Speed Channel or 550 whichever is less.

Maximum α - Factor allowed on SHC is given by:

$$650 - 0.25I$$

(where I = total IMTAC value on PAC, see Appendix B, 3.0.6)

4.0 EXECUTIVE

4.0.1 The following Executives may be used with a 1904A:

Unpaged system or paging switched OFF	Paged system with paging switched ON
E6BM	EWG4 (with GEORGE 4)
E6RM	
EWG3 (with GEORGE 3)	

For further details of Executive, including compile-time options, store occupancy and peripheral requirements see Section 2.

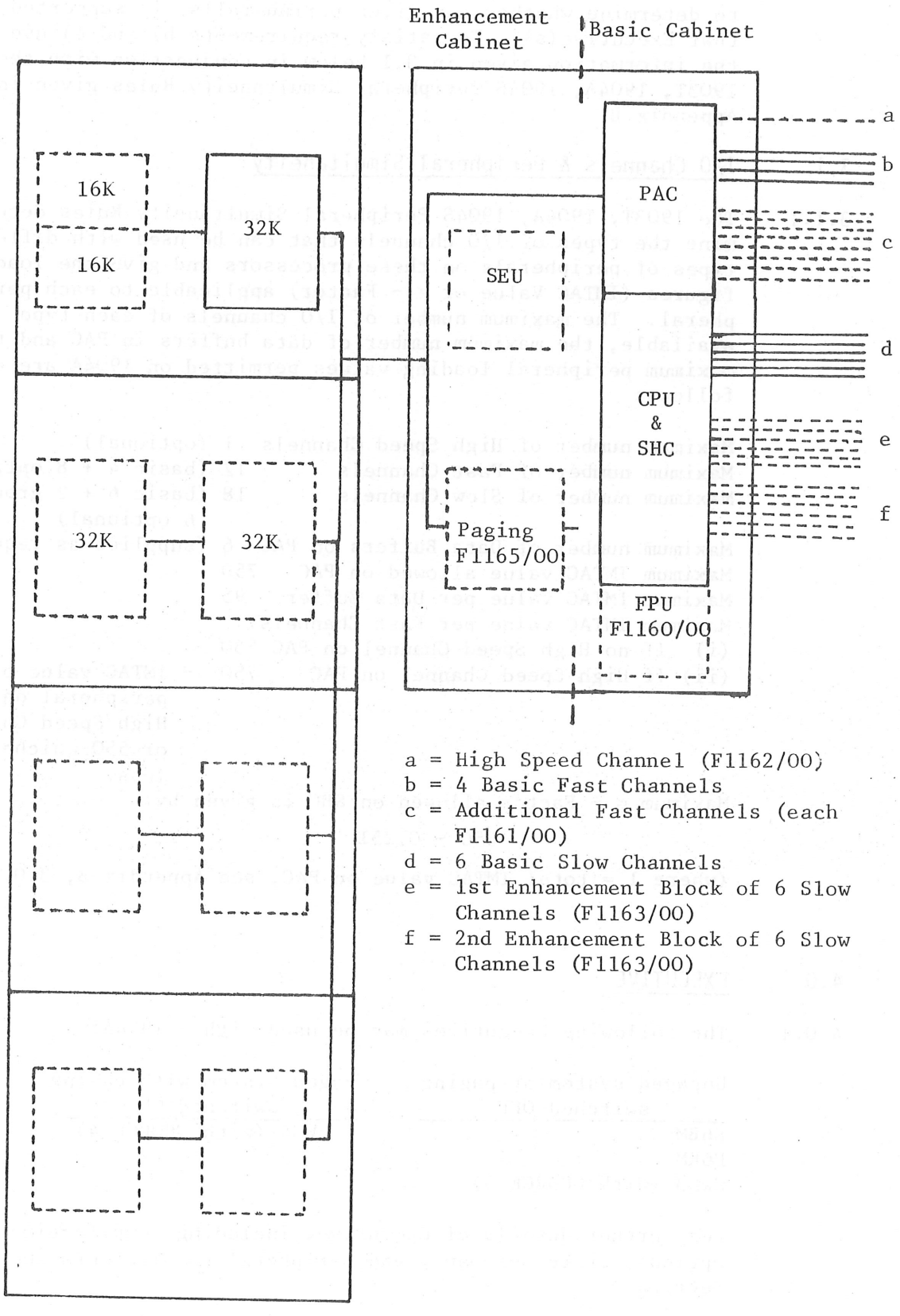


Figure 1 Logical Structure of 1904A

5.0 HARDWARE GENERAL DESCRIPTION

5.1 System Description

5.1.1 The CPU, PAC, and all optional features are implemented in TTL technology and all with the exception of the Paging Feature and a Store Extension Unit are housed in a 2-bay cabinet structure. The latter are housed in a Central Processor Extension Cabinet which forms a third bay. The core store is housed in separate store cabinets, each capable of holding up to 64K words.

5.1.2 The processor/store interface is effectively 25 bits wide, 24 bits + parity, and access can only be made to one store location at a time. The logical structure of the system is shown in Figure 1.

5.2 Central Processor

5.2.1 The 1904A Central Processor is store image compatible with 1903T, 1904S, 1904E/F and 1906 in respect of data and instruction formats and implements the 1900 Series order code to C2 level. For list of instructions and timings see 8.0 Performance. Hardware Accumulators, Real Time Clock and Mill Timer are all provided as standard.

There are two versions of 1904A Central Processor, early machines up to Serial Number 470 are known as Mark 1 machines, those from Serial Number 471 onwards are known as Mark II machines. The differences mainly affect the enhanceability to 1904S and the fitting of a Paging Feature. For details see 7.0.

5.2.2 REAL TIME CLOCK

The Real Time Clock enables Executive to output the date and time on all console messages, is used by GEORGE for scheduling and logging purposes and enables the GIVE instruction to be used to obtain the date and time as required by programmers.

Resolution = 200 Milliseconds

5.2.3 MILL TIMER

The Mill Timer (also called Program Timer) counts machine beats on clock pulses into a hardware register while the processor is in Object Program Mode. It does not count any beats due to processing within the Floating Point Unit although it counts those beats due to any fixed point instruction which is proceeding simultaneously. It does not count during extra codes or hesitations. When the register is almost full the contents are added to the clock count for that particular program held by Executive. The Executive message CLOCKED NN refers to millions of clock pulses and not seconds. In order to obtain an estimate in seconds for the 1904A the CLOCKED NN figure should be halved.

Thus CLOCKED NN x 0.5 ≃ PP seconds.

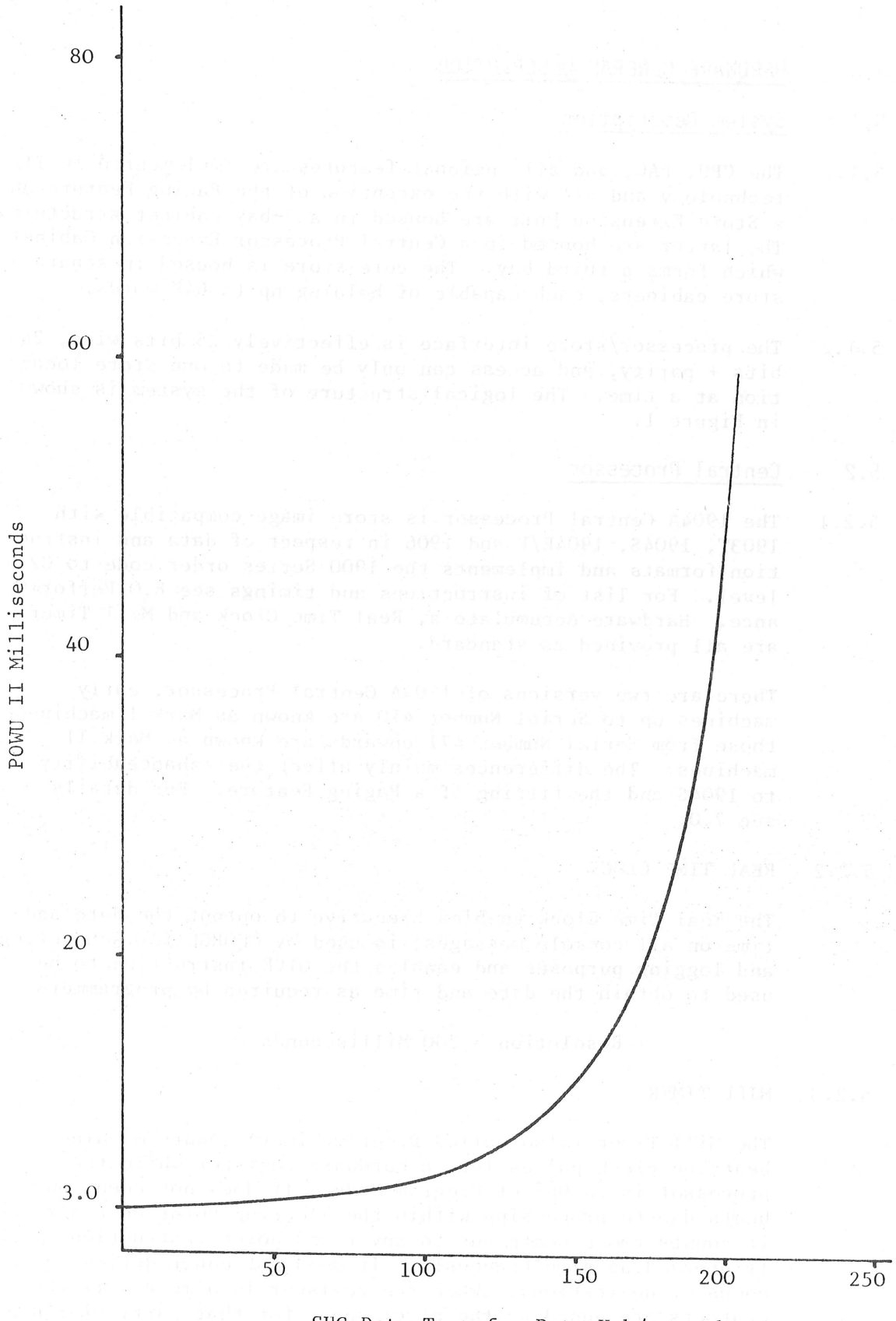


Figure 2 1904A Performance Degradation Due To SHC Activity

5.2.4 PERIPHERAL HANDLING

Peripheral data transfers are handled by either the SHC or PAC depending on the peripheral type (see Appendix B, 1903T, 1904A, 1904S Peripheral Simultaneity Rules) and information concerning:

(a) the number of outstanding units of transfer,
(b) the absolute address of the next unit, and
(c) the style of transfer

are held in control words, which are read and updated once for each unit of data written to or read from main store. The four characters of a burst from a burst-mode peripheral are assembled into one word before being presented to main store.

5.2.5 SLOW HESITATION CONTROL

The SHC is an integral part of the CPU and the CPU mill is used to update the control words which are held in main store. The processor's B-register is used to assemble 4-characters serially into one word during a burst-mode transfer. For these reasons a data transfer via SHC and instruction processing cannot go on simultaneously and a peripheral request for data transfer must wait until the processor's mill and registers are in a condition to deal with the request. After such a delay the processing of instructions will hesitate for the duration of the transfer. The maximum CPU delay and SHC hesitation times, assuming no interference from PAC which has priority for main store access, are given below:

Type of Hesitation	Nominal Time in microseconds Input	Output
Single Character Single Channel	7.9	7.9
Four Character Single Channel	14.0	13.5
Single Character Multi Channel	Add 2.0	
Four Character Multi Channel	Add 2.0	
Control Word Recharge	Add 2.4	
Scatter read-gather write	Add 3.4*	
Maximum CPU delay	7.0	(Average 3.0)

*Only when the paging feature is used and when a page boundary is crossed.

The effect of data transfers via the SHC on processor performance is indicated in Figure 2.

5.2.6 PERIPHERAL AUTONOMOUS CONTROL

The PAC is an autonomous unit having direct access to main store, a mill to update the control words, control word buffers and data buffers. Its logical structure is shown in Figure 4 below. The control word buffers and data buffers are supplied as required; one pair of control word buffers per channel connected, High speed data buffers and up to 6 Fast data buffers depending on the number and type of peripherals connected. Since PAC has priority for store access, the processor will be forced to hesitate when a clash occurs,

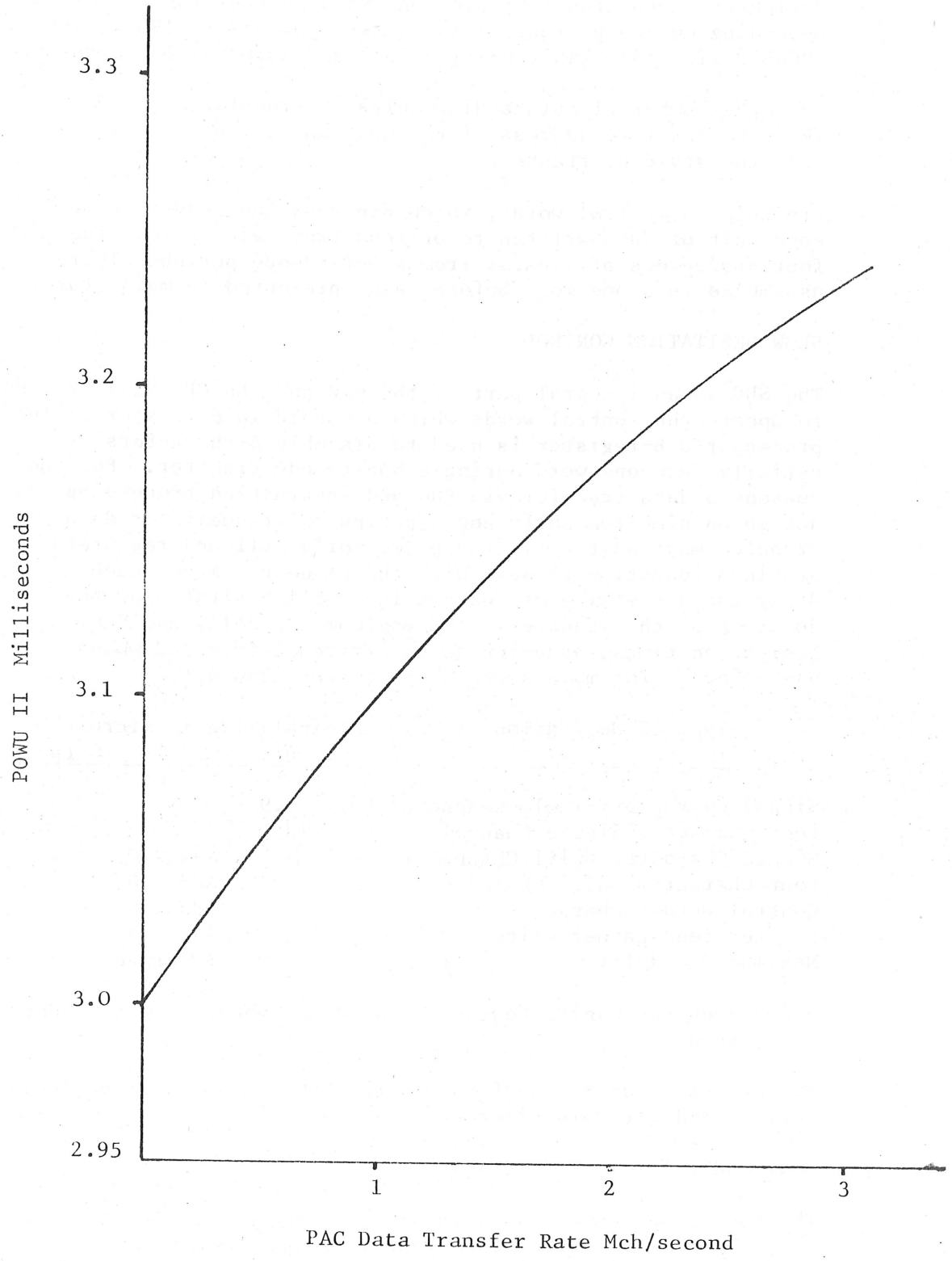


Figure 3 1904A Performance Degradation Due To PAC Activity

consequently instruction processing may be held up or SHC hesitations may be interrupted. However, since many operations in the central processor do not involve the store, the average delay experienced by the processor will be significantly less than the maximum and is taken into account in calculating the degradation in processor performance due to PAC activity illustrated in Figure 3. The simultaneity rules take account of the effect of PAC on SHC timings.

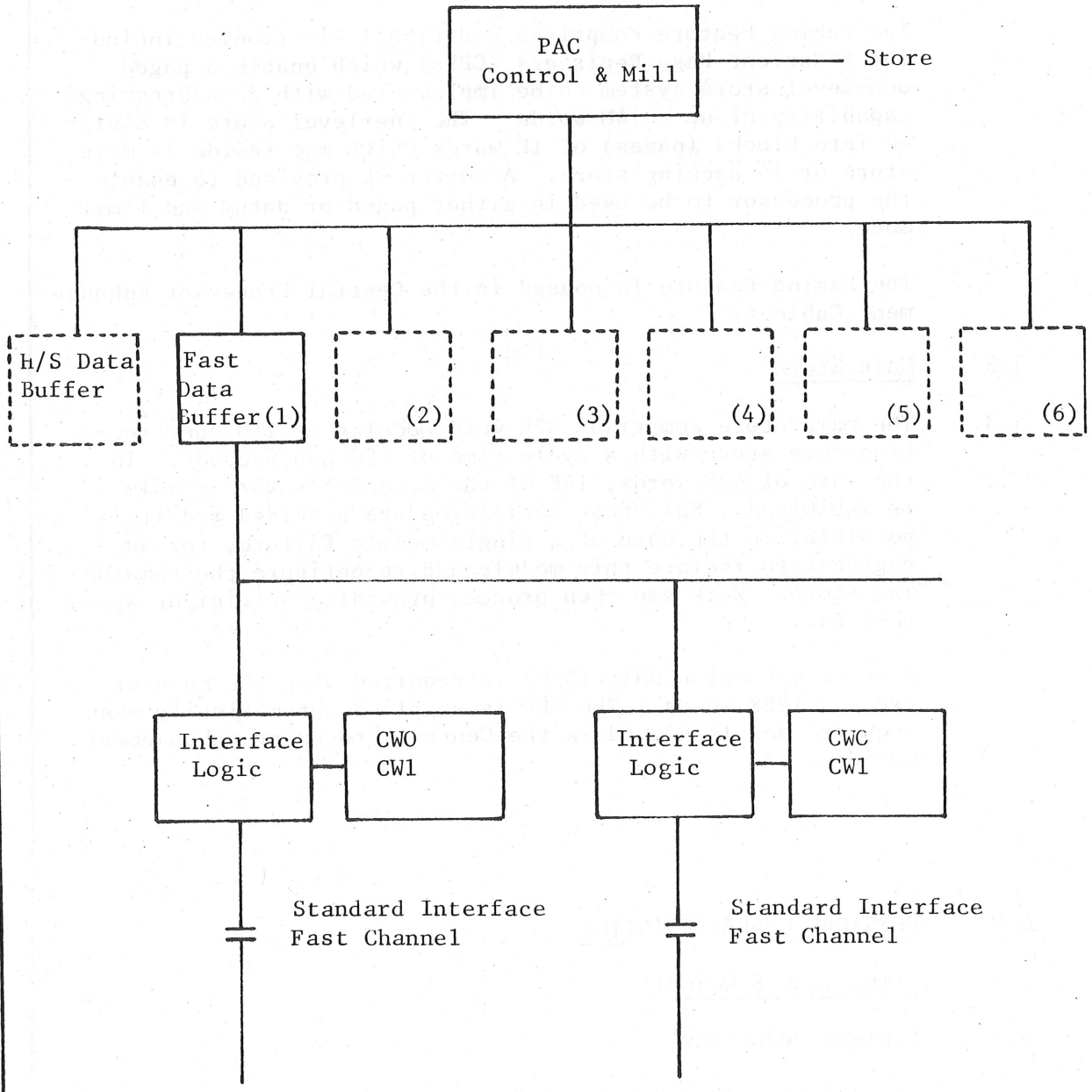


Figure 4 Logical Structure of 1904A PAC

5.2.7 FLOATING POINT UNIT (F1160/00)

The Floating Point Unit comprises additional electronics including a hardware floating point accumulator. It operates autonomously with the CPU during the execution phase of floating point instructions and provides results identical to those obtained with the Floating Point Units on 1907, 1905F, 1903T and 1904S. For list of instructions and timings see 8.3.

5.2.8 PAGING FEATURE (F1165/00)

The Paging Feature comprises additional electronics including 8 Current Page Registers (CPRs) which enable a paged one-level store system to be implemented with an addressing capability of up to 4M words. The one-level store is divided into blocks (pages) of 1K words which may reside in main store or in backing store. A switch is provided to enable the processor to be used in either paged or datum and limit mode.

The Paging Feature is housed in the Central Processor Enhancement Cabinet.

5.3 Main Store

5.3.1 The main store comprises 32K word modules of 2½D construction core store with a cycle time of 750 nanoseconds. In the case of 48K words, 16K of the second 32K word module is inhibited. Self-test facilities are provided and it is possible, in the case of a single module failure, for an engineer to isolate this module and reconfigure the remaining store. Work can then proceed providing sufficient store remains..

A Store Extension Unit (SEU) is required when the main store exceeds 128K words. The SEU is supplied automatically when required and is housed in the Central Processor Enhancement Cabinet.

6.0 PHYSICAL CHARACTERISTICS

6.1 Dimensions & Weight

6.1.1 CENTRAL PROCESSOR

Dimensions

Height 55" (1400mm)
Depth 28½"(720mm)
Length 101½"(2568) Basic Processor
140" (3556mm) With Extension Cabinet

Access Clearance	Front	54" (1370mm)
	Rear	54" (1370mm)
	Left	-
	Right	36" (910mm)
Weight		1300 lbs (520Kgs) Basic Processor 1500 lbs (681Kgs) With Extension Cabinet.

6.1.2 MAIN STORE CABINET

Dimensions	Height	55" (1400mm)
	Depth	28½" (720mm)
	Length	56" (1425mm)
Access Clearance	Front	54" (1370mm)
	Rear	54" (1370mm)
	Left	36" (910mm)
	Right	36" (910mm)
Weight		800 lbs (364Kgs)

6.1.3 CONSOLE TYPEWRITER DESK

Dimensions	Height	29" (740mm)
	Depth	25½"(650mm)
	Width	36" (1830mm)
Access Clearance	Operational clearances (see 6.5)	
Weight		300 lbs (136Kgs)

6.1.4 EXTENSION CONSOLE DESK

Dimensions	Height	29" (740mm)
	Depth	25½"(650mm)
	Width	36" (914mm)
Access Clearance	Operational clearances (see 6.5)	
Weight		200 lbs (91Kgs)

6.2 Mains Supply

A Motor Alternator is mandatory. This may be either 1986/02 (45KVA) or 1986/07 (65KVA) depending on the total system requirements.

In either case the mains supply required will be 3 phase 50Hz.

6.3 Power Requirements & Heat Dissipation

6.3.1 Power Required

Central Processor		4.1 KVA
Main Store	32K	2.0 KVA
	64K	3.5 KVA
T/W Consoles		0.4 KVA

6.3.2 Heat Dissipation

Central Processor		3.0 KW
Main Store	32K	1.6 KW
	64K	2.8 KW
T/W Consoles		0.3 KW

6.4 Environment

Temperature range	$10^{o}C$ - $35^{o}C$
Relative Humidity	20% - 80%
Air Cleanliness	Air filtering not required under normal office conditions

6.5 Site Layout

6.5.1 The possible relative positions of the Central Processor, Main Store and Console Typewriter Desk are determined by the physical space available, cable lengths, access clearance required and the operational requirements of the system as a whole. CED Environmental Engineering must be consulted regarding all site layouts and can advise on the best layout taking into account all the relative factors.

The details given below are for guidance only:

6.5.2 CABLE LENGTHS

	Standard	Other*
Processor - Store	14' (4.26M)	20' (6.1M)
Processor - C/TW Desk	45' (13.73M)	Up to 100' (30.5M)
C/TW Desk - Extension Desk	The normal length cable supplied allows the Extension Desk to be positioned immediately to the right of the Console Desk. For a remote position, cables of length 20' (6.1M) are available allowing the Extension Desk to have a physical separation of 15' (5M) to the right or 10' (3M) to the left of the Console Desk.	

*Where non-standard cables are required they will be ordered from Production by CED. The use of other than the standard 14' Processor-Store cables will degrade the system performance, see Section 8 for details.

6.5.3 STANDARD LAYOUTS

See Figure 5 opposite

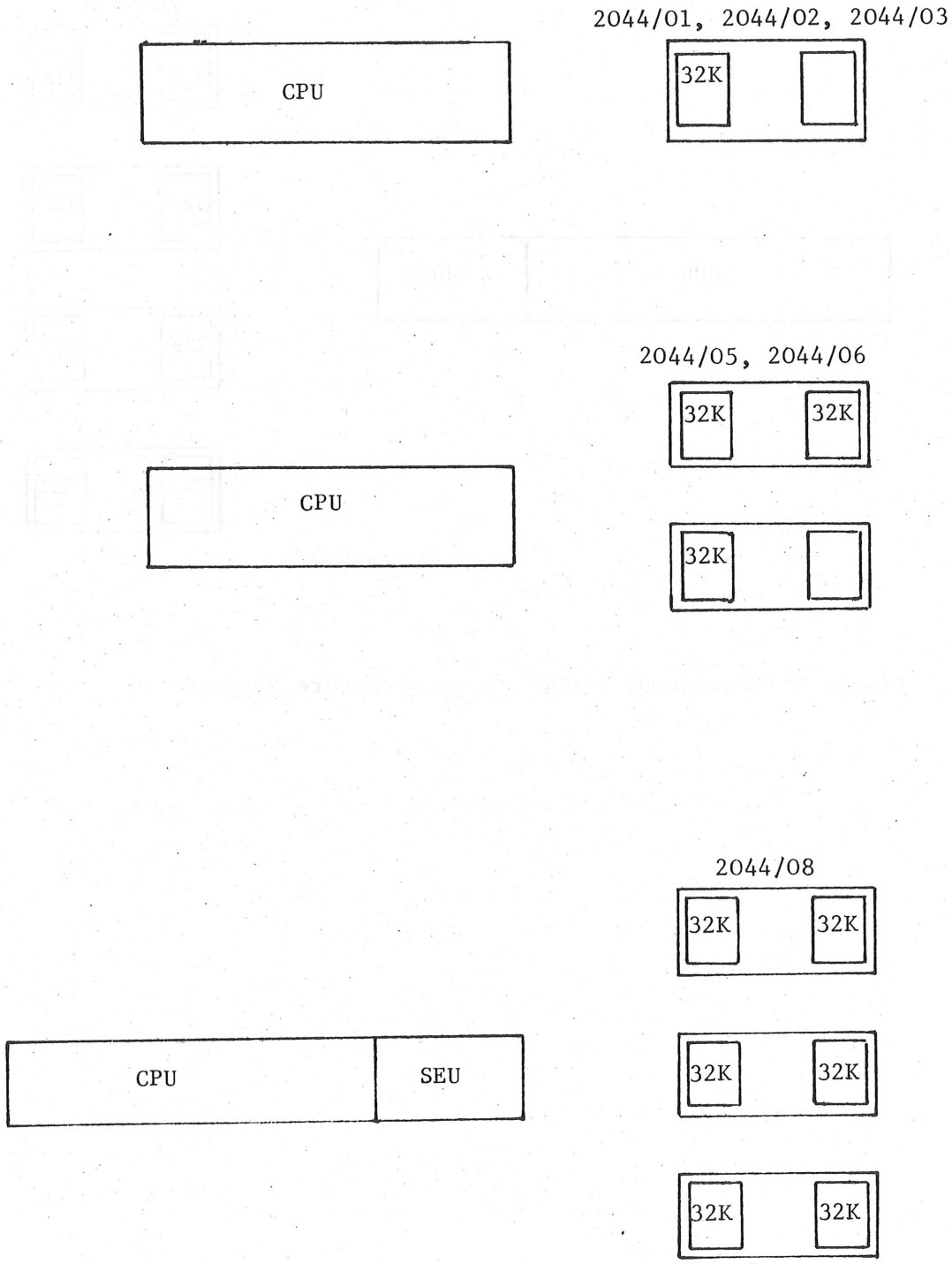


Figure 5 1904A Processor/Store Layouts

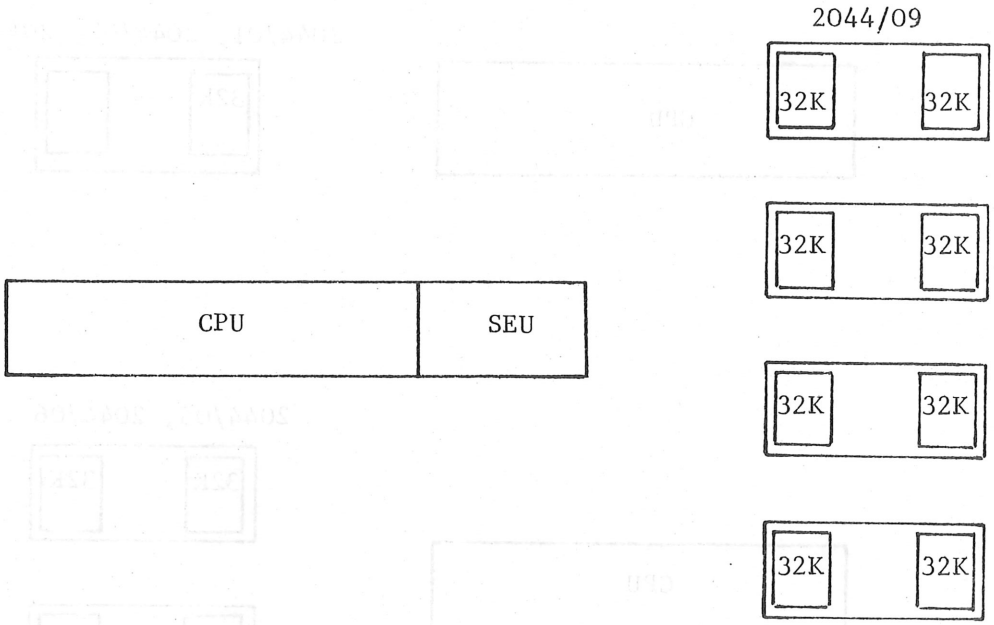


Figure 5 (Continued) 1904A Processor/Store Layouts

7.0 FIELD ENHANCEMENTS

The information given here is for guidance only on what is involved in fitting each enhancement. Further details, including estimates of system down-time, testing time, etc. must be obtained from CED. Where the change to the system necessitates ordering a new issue of Executive this is explicitly stated.

7.1 F1160/00 Floating Point Feature

This feature comes as a logic plane complete with packages, cableforms and fittings. In addition there are 3 packages to replace 3 blank packages already fitted to the machine.

Fitting involves replacing a blank logic place (already fitted to the machine) by the new logic plane, making all cableform connections, replacing the 3 blank packages by the new packages and fitting new marker strips, coding buttons, etc.

7.2 F1161/00 Fast Peripheral Channel

Fitting involves adding the Fast Channel interface socket and a number of packages (the quantity depends on whether or not a Data Buffer is required), revising the package coding buttons and modifying the PAC Plane back wiring (priority) depending on the revised peripheral configuration.

A new Executive must be ordered to support the new peripheral configuration.

7.3 F1162/00 High Speed Peripheral Channel

Fitting involves adding the High Speed Channel interface socket and making connections to the PAC Plane, replacing 7 packages, adding 2 additional packages and revising the package coding buttons.

A new Executive must be ordered to support the revised peripheral configuration.

7.4 F1163/00 Group of 6 Slow Channels

Fitting involves adding the Slow Channel interface sockets and packages and connecting the channels to the corresponding positions on the Distributor Plane.

A new Executive must be ordered to support the revised peripheral configuration.

7.5 F1165/00 Paging Feature (MKII Machines Only)

This feature comes as a logic plane assembly with packages, cableforms and fittings and an Engineer's Control Panel and Monitor Panel. Also included is a 1904A Processor Enhancement Cabinet if not already fitted to the machine.

ENHANCEMENT CABINET ALREADY FITTED

Fitting the paging feature involves replacing a blank logic plane by the new logic plane, fitting the Engineers Control Panel and Monitor Lamp Panel, making the cableform connections and replacing blank packages in the distributor plane by new packages. Revising coding buttons etc.

NO ENHANCEMENT CABINET FITTED

Fit enhancement cabinet containing the paging feature logic plane, Engineer's Control Panel and Monitor Panel. Make all cableform connections, replace blank packages in distributor plane and revise coding.

Order Executive EWG4 and GEORGE 4.

NOTE: F1165/00 cannot be field fitted to MK1 1904A's (i.e. machine numbers less than 471).

7.6 C1050/00 Conversion of 2044/01 to 2044/03

This conversion involves fitting an additional 32K Store Module in the existing Store Cabinet, making cableform connections to the existing Store Module and the Power Distribution Unit and modifying wire links on a package in the Distributor Plane.

7.7 C1051/00 Conversion of 2044/03 to 2044/05

This conversion involves adding a Store Cabinet, fitting a 32K Store Module into the cabinet, making cableform connections, modifying 2 wire links and fitting 2 new packages in the Distributor Plane.

7.8 C1052/00 Conversion of 2044/05 to 2044/06

As for 7.6 above, except that the additional 32K Store Module is fitted into the existing 2nd Store Cabinet.

7.9 C1053/00 Conversion of 2044/06 to 2044/08

This conversion involves adding a Store Cabinet and fitting 2 32K Store Modules into it, making cableform connections, adding an Enhancement Cabinet (containing an SEU) to the CPU and modifying the Distributor Plane.

7.10 C1054/00 Conversion of 2044/08 to 2044/09

As for 7.9 above, except that the Enhancement Cabinet (containing the SEU) is already fitted to the CPU.

7.11 Conversion of 1904A to 1904S

The conversions C1176/01 and C1176/02 apply only to the 1904A CPU (2044/00); they do not include replacement of the 1904A Core Store by 1904S MOS Store. Store replace-

ment can be carried out after each conversion, if required, by ordering the appropriate size of MOS Store and withdrawing the original Core Store.

There are therefore several versions of systems arrived at by conversion from 1904A, depending on the MARK of 1904A converted and whether or not the store is replaced. Mark 1 processors cannot be converted to Mark 2 processors and can be regarded as "reduced facility machines" when converted to any interim version of 1904S. The symbol * is used to denote converted 1904A systems which retain core store. The various processors and systems may be summarised as follows:

Processor Name

1904A Mark 1 =	2044/00 CPU's up to and including Machine No. 470
1904A Mark 2 =	2044/00 CPU's later than Machine No. 470
1904A Mark 1+C1176/01 =	2046/00 CPU Mark 1
1904A Mark 2+C1176/02 =	2046/00 CPU Mark 2

System Name

1904A =	Any 1904A system, Mark 1 or Mark 2, all have Core Stores
1904S * Mark 1 =	1904A Mark 1+C1176/01 + retained Core Store
1904S * Mark 2 =	1904A Mark 2+C1176/0 + retained Core Store (See Note 3)
1904S Mark 1 =	1904A Mark 1+C1176/01 + store replacement (See Note 2)
1904S =	1904A Mark 2+C1176/02 + store replacement

The latter is the same as a full specification 1904S; for details see page 540.1.

For details of 1904S*Mark 1, 1904S*Mark 2 or 1904S Mark 1, see page 530.1.

NOTE 1. All 1904S systems ordered as 1904S systems are Mark 2 machines, that is all have Machine Numbers higher than Machine No. 471. However due to non-availability of MOS Store to meet early 1904S deliveries some "Interim 1904S Systems" were delivered; these are equivalent to 1904S*Mark 2.

2. To date none of these systems exist, i.e. no converted 1904A Mark 1 has also had its Core Store replaced by MOS Store. The store replacement is not therefore recommended, as a system test would be required, and in any case the cost of store replacement would be difficult to justify because of the marginal improvement in performance.

3. The work involved in converting to this system depends on the mod level of the 1904A Mark 2. In many cases

the full conversion to 1904S may be easier. The full conversion to 1904S, i.e. also replacing the store, is recommended.

7.11.1 C1176/01 Conversion of 2044/00 Mark 1 to 2046/00 Mark 1

This conversion involves replacement of packages in planes 2, 3 and 6, revising the coding buttons and modifying the polarising of the Burndy sockets on planes 2, 3 and 6. In all 45 packages are replaced in the CPU.

7.11.2 C1176/02 Conversion of 2044/00 Mark 2 to 2046/00 Mark 2

This conversion involves adding an enhancement cabinet if not already fitted, replacement of packages in planes 2, 3 and 6, modifying a plane carrier frame in the enhancement cabinet and adding additional packages and replacing a number of cableforms depending on the size of store on the system. The work involved also depends on the mod level of the CPU. The Extension Console Typewriter Desk is modified to include the Store Reconfiguration Controls.

7.12 Replacement of Core Store by MOS Store

See "Reduced Facility 1904S" entry page 530.1.

8.0 PERFORMANCE

8.0.1 All instruction times and work mix times quoted apply to instructions or work mix programs held in even numbered store blocks on 1904A systems without Store Extension Units (SEUs) and with standard 14' cables between the Central Processors and stores. The times quoted may be degraded due to the addition of an SEU, the use of longer store cables or for instructions held in odd numbered store blocks by the percentages given below, except where explicitly stated otherwise:

a) Less than 4% if an SEU is fitted.

b) Less than 2% due to the use of 20' store cables.

c) Less than 4% for odd numbered store blocks.

All tolerances, where given, and degradation figures, where applicable, are additive.

8.1 Work Mixes

The times quoted are subject to a machine tolerance of ±5% plus an additional tolerance of +1% -2% due to the method of measurement being dependent on the 50Hz mains frequency at the time the measurements are taken. See also 8.0.1 above.

Post Office Work Unit II (POWU II)

Basic 1904A	3.0	milliseconds
Paging Switched OFF	3.4	"
Paging Switched ON	3.8	"

GAMM Mix (with F1160/00 fitted)

Non-paged machine	11.0	microseconds
Paging Switched OFF	12.0	"
Paging Switched ON	13.0	"

8.2 Fixed Point Instruction Times

8.2.1 The instruction times quoted below are subject to a tolerance of ±10%. The timings may be further degraded as follows:

a) By the figures given in Section 8.0.1 above.

b) For paged machines by up to 2% due to the variable overheads of loading the current page registers.

c) By an additional tolerance of +1% -2% due to the method of measurement depending on the mains frequency.

All times are applicable to 15 bit and 22 bit address modes of working.

FUNCTION	TIMING UNMODIFIED Microseconds	TIMING MODIFIED Microseconds
000	2.6 (2.2)	3.1 (2.7)
001	2.6	3.1
002	2.6	3.1
003	2.6	3.1
004	2.6	3.1
005	2.6	3.1
006	2.6	3.1
007	2.6	3.1
010	2.6	3.1
011	3.1	3.6
012	2.6	3.1
013	3.1	3.6
014	2.6	3.1
015	3.1	3.6
016	2.6	3.1
017	3.1	3.6
020	2.6	3.1
021	2.6	3.1
022	2.6	3.1
023	1.5	2.0
024	2.6	3.1
025	2.6	3.1
026	2.6	3.1
027	2.6	3.1
030	3.1	3.6
031	3.1	3.6
032	3.1	3.6
033	2.6	3.1
034	3.1	3.6
035	3.1	3.6
036	3.1	3.6
037	3.1	3.6
040	15.0 - 16.0	15.5 - 16.5
041	15.0 - 16.0	15.5 - 16.5
042	15.0 - 16.0	15.5 - 16.5
043	7.0	7.5
044	16.0 - 17.0	16.5 - 17.5
045	17.8 - 19.0	18.3 - 19.5
046	16.4 - 17.4	16.9 - 17.9
047	13.1	13.6
050	2.5	-
052	2.5	-
054	2.5	-
056	2.5	-

FUNCTION	TIMING UNMODIFIED Microseconds	TIMING MODIFIED Microseconds
060	2.5	-
062	2.5	-
064	2.5	-
066	2.5	-
070	3.0	-
072	3.0	-
074	2.0	-
076	2.0	-
100	2.5 (2.0)	2.5 (2.0)
101	2.5	2.5
102	2.5	2.5
103	2.5	2.5
104	2.5	2.5
105	2.5	2.5
106	2.5	2.5
107	2.5	2.5
110	2.5 + 0.5N	-
112	2.0 + 0.5N	-
114	3.0 + 0.5N	-
116	8.4 + 4.8N	-
111	3.0 + 0.5N	-
113	3.0 + 0.5N	-
115	5.0	-
117	3.1	3.6
120	2.5	-
121	2.5	-
122	2.5	-
123	2.0	-
124	6.0	-
136	2.5	-
126	7.3 + 1.8N	-
127	3.5 + 1.2N	-

N = Number of places shifted, moved or normalised.

8.3 Floating Point Instruction Times

8.3.1 The instruction times quoted below apply only to 1904A systems fitted with the F1160/00 Hardware Floating Point Unit. It is possible for both fixed point and floating point functions to be executed simultaneously. There are up to 4 phases applicable to floating point instructions and only phase 4 is capable of overlap.

8.3.2 In phase 1 the instruction is fetched from store by the central processor; in phase 2 the N address is modified; in phase 3 the central processor loads the operand into the floating point unit (or unloads the operand into

store), and in phase 4 the floating point unit executes the instruction. As soon as phases 1, 2 and 3 have been completed the central processor is free to continue with fixed point instructions or to execute phases 1, 2 and 3 of another floating point instruction (there is a buffer available in the floating point unit to queue a second floating point order). If phase 4 of the first instruction is still in progress and a third floating point instruction is encountered it will be executed to the end of phase 2 and thecentral processor will be held up until phase 4 of the first floating point instruction is completed. Since none of the 076, 136 or 137 instructions involve the floating point unit in any actual calculation, there can be no overlap for any instructions that follows them but if a 076, 136 or 137 instruction follows one of the other floating point orders, then overlap applies in the normal way.

8.3.3 The timings in microseconds for phases 1, 2 and 3 are as follows:

	Basic 1904A	Paging OFF	Paging ON
Phase 1 Fetch Instruction	1.51	1.65	1.72
Phase 2 Modification	0.50	0.50	0.50
Phase 3 Load Operand	1.85	2.13	2.51
Phase 3 Unload Operand	3.26	3.26	3.56

An SEU will not degrade the above times by more than:

For degradation due to odd numbered store modules or the use of longer than the standard 14' cables see 8.0.1.

All above times are subject to a tolerance of ±10%.

8.3.4 Phase 4 timings are not subject to any degradation due to the use of non-standard length store cables or paging. They are however subject to a machine tolerance of ±5% plus an additional tolerance of +1% -2% due to mains frequency variation.

Timings in microseconds are as follows:

FUNCTION	130	131	132	133	134	135	136	137
MIN/U	-	2.0	3.0	3.0	10.0	22.5	-	-
MAX/U	-	25.5	9.5	9.5	10.5	25.0	-	-
MIN/N	2.5	-	4.0	4.0	11.0	23.0	-	-
MAX/N	26.0	-	28.0	28.0	47.5	42.5	1.0	1.0

MIN = Minimum calculation (no rounding, correction or alignment required)
MAX = Maximum calculation (rounding, correction and alignment required)
/U = Un-normalised operand (no normalising required)
/N = Normalised operand (normalising required)

8.4 I/O Performance

The figures given below are maximum data transfer rates and are given as general information only. They cannot be used as the basis of checking peripheral simultaneity because this depends on worst case maximum peripheral data transfer rates, crisis time considerations, the effect of PAC transfers on the SHC and other factors beyond the scope of this manual. The actual data transfer rate achieve on any system depends on the peripheral configuration, the connectivity to the system and the program(s).

Maximum I/O Throughput per system:

a) With a High Speed Channel used on PAC 3.0 Mch/second
b) Without a High Speed Channel on PAC 2.2 Mch/second

Maximum data transfer rate of:

a) High Speed Channel 1.5 Mch/second
b) Fast Channel (or PAC Data Buffer) (See Note 1) 380 Kch/second
c) Slow Channel (See Note 2)
   i) Burst Mode (4-Character) 80 Kch/second
   ii) Single Character 30 Kch/second

NOTE 1: More than one Fast Channel may be connected to a PAC data buffer therefore the maximum data transfer rate of all Fast Channels sharing one data buffer is 380 Kch/second.

2: The maximum data transfer rate of a Slow Channel is the same as rhat for the SHC as a whole which is given by:

$$\frac{10^6}{\text{Hesitation Time in microseconds}}$$ (See 5.2.5)

However, because SHC activity heavily degrades the processor performance and is itself degraded by PAC activity it would not be sensible to allow fast peripherals to be connected via the SHC Slow Channels. The data transfer rates given for Slow Channels are not therefore the maximum imposed by the hardware but are a guide to the practical limits that are imposed. The Simultaneity Rules determine whether any given peripheral may be connected via a Slow Channel or not.

9.0 ORDER VETTING CHECKLIST

NEW SYSTEM ORDERS

1. Check that the configuration includes all mandatory peripherals required for maintenance purposes and by Executive and/or Operating System. See 9.1 and Section 2.

2. Check that the correct type of Motor Alternator has been specified. See 6.2.

ENHANCEMENT ORDERS

3. Check that the correct system number has been quoted.

ALL ORDERS

4. Check that all peripherals specified are supported by the Executive to be used on the System. See Appendix A.

5. Check peripheral simultaneity and that the correct quantity and types of I/O channels have been specified for the connection of all peripherals. See 3.1 and Appendix B.

6. Where peripheral switches have been specified check that a switching diagram has been included.

7. When peripherals have been retained from some earlier system or from other sources check that these are listed on the specification form.

8. Check that a diagram of all communications configurations is included on the Communications Specification Form.

9. See appropriate peripheral ORDER VETTING CHECKLISTS for dependencies, features, etc. applicable to the peripherals or peripheral sub-systems.

9.1 Mandatory Peripherals Required for Maintenance Purposes

It must be possible to have at least one suitable input device and one suitable output device connected to a system for maintenance purposes. Either these must be permanently connected to the processor or it must be possible to switch them to the processor by means of Standard Interface Switching Units. The only input devices suitable are either:

a) An 80 column card reader - with out without Card Image

or

b) A paper tape reader capable of handling ISO 8 channel tape.

The only output devices suitable are either:

a) A line printer with 96 or more print positions, buffered or unbuffered and connected to either PAC or to SHC.

or

b) A paper tape punch, provided there is on the customer's premises an off-line printer which can accept the paper tape produced by this punch.