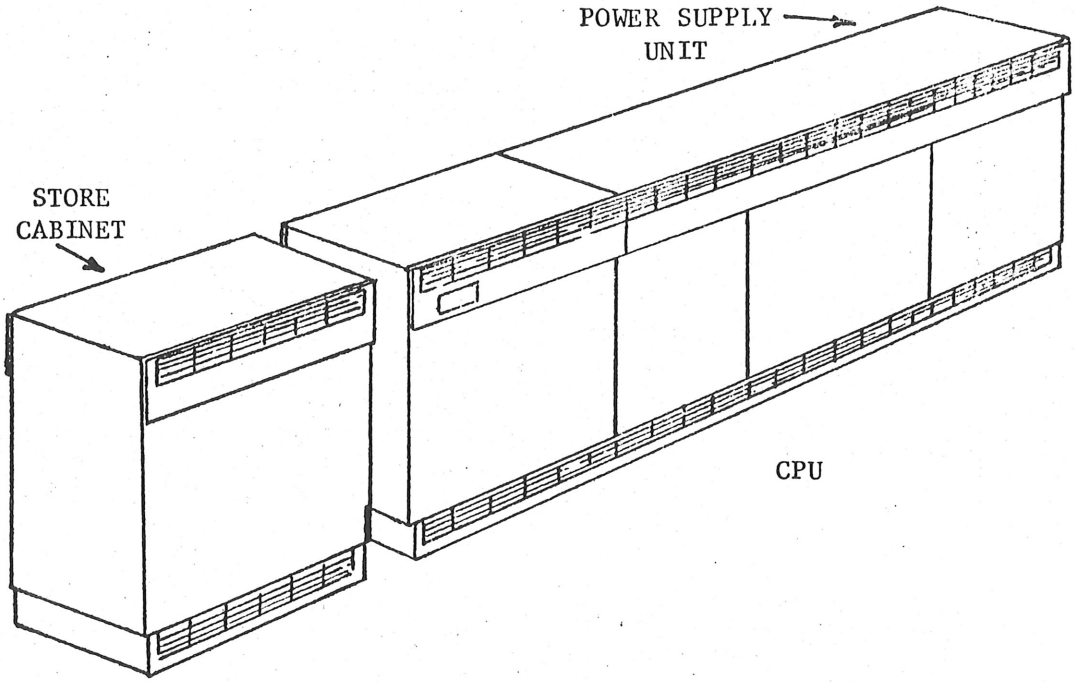
Reduced Facility 1904S Systems



1.0 INTRODUCTION

1.0.1 The systems described here do not meet the full 1904S specification. These are:

1. Interim 1904S systems supplied to meet early 1904S deliveries at the time MOS Stores were unobtainable. These systems comprise a 1904S CPU + 1904A Core Store and have been referred to as "Interim 1904S" or 1904S*.

2. Systems derived due to enhancement of 1904A Mark 2 by the addition of C1176/02. These systems are referred to as 1904S* Mark 2 and are identical to the Interim 1904S or 1904S*.

3. Systems derived due to enhancement of 1904A Mark 1 by the addition of C1176/01 and are referred to as 1904S* Mark 1.

There is one further possible type of system that could be derived by replacement of the Core Store on a 1904S* Mark 1 by MOS Store and is referred to as 1904S Mark 1. However none of these exist and such a system would, if ever required, be subject to a full Systems Compatibility Test.

NOTE: A 1904S* Mark 2 (or 1904S*) can be enhanced to the full 1904S specification by replacement of the Core Store by MOS Store. For details of 1904S see page 540.1. A Mark 1 machine cannot be enhanced to a Mark 2 machine and cannot therefore be enhanced to the full 1904S specification.

The main differences between Mark 1 and Mark 2 systems are that the Mark 2 systems can have the features listed below but the Mark 1 systems cannot have them.

Interrupt on Store Parity Failure)
Store Reconfiguration) Standard

2nd PAC (F1389))
Paging Feature (F1165/00)) Optional but mutually exclusive

1.0.2 The Reduced Facility 1904S Systems can be summarised as follows:

System Name

1904S* Mark 1 = 1904A Mark 1 + C1176/01 + retained Core Store
1904S Mark 1 = 1904A Mark 1 + C1176/01 + MOS Store (never implemented)
1904S* Mark 2 = 1904A Mark 2 + C1176/02 + retained Core Store = 1904S*

1.1 Summary of Characteristics

Order Code Level (all systems)		C
Main Store Cycle Time -	1904S* Mark 1)	750 Nanoseconds (as 1904A)
	1904S* Mark 2)	
	1904S Mark 1	500 Nanoseconds (as 1904S)
POWU II -	1904S* Mark 1, 1904S* Mark 2	2.4 Milliseconds
	1904S Mark 1 (estimated)	2.3 Milliseconds (as 1904S)
GAMM Mix (All systems with F1160/00 fitted)		10.5 Microseconds (as 1904S)
Total I/O Throughput -	1904S* Mark 1,)	3.0 Mch/second (as 1904A)
	1904S Mark 1)	
	1904S* Mark 2	5.0 Mch/second (as 1904S)

2.0 TYPE NUMBERS & CONSTITUENT ITEMS

2.1 Standard Components

Type Number	Description
2046/00 Mark 1 =	2044/00 + C1176/01. Description as for 2044/00, see page 520.1, except that the CPU data flow has been speeded up by the substitution of packages with Schottky TTL Integrated Circuits replacing standard TTL Integrated Circuits where necessary.
2046/00 Mark 2 =	2044/00 + C1176/02. Description as for 2046/00, see page 540.1.
2044/05-2044/09	96K-256K words 750Nsec. Core Store
or	
2046/05-2046/09	96K-256K words 500Nsec. MOS Store

2.2 Optional Hardware Features

The following items may be field fitted:

Type Number	Description	
F1160/00	Floating Point Unit	
F1161/00	Fast Peripheral Channel	See Note 1
F1162/00	High Speed Channel	See Note 2
F1163/00	Group of 6 Slow Channels	Maximum 2
F1165/00	Paging Feature)	See Note 3
F1389/00	2nd PAC)	
F1900/00	Main Store Switching Feature	See Note 4

NOTES: 1. Mark 1 systems or Mark 2 with 1 PAC - maximum 8
Mark 2 systems + 2nd PAC (F1389) - maximum 14

2. Mark 1 systems or Mark 2 systems with 1 PAC - maximum 1
Mark 2 systems + 2nd PAC (F1389) - maximum 2

3. Mark 2 only. Features are mutually exclusive

4. May be added to any adjacent pair of 1904S systems with MOS Store.

2.3 Conversions

For Core Store conversions see page 520.2.

For MOS Store conversions see page 540.2.

A 1904S* Mark 1 may be converted to 1904S Mark 1 by replacing the store, but see 1.0.1.

A 1904S* Mark 2 may be converted to 1904S by replacing the store.

3.0 CONNECTIVITY

The connectivity of all systems is the same as for 1904S, see page 540.2. The only exception is that Mark 1 systems cannot have a 2nd PAC and are therefore limited to a maximum of 1 High Speed Channel and 12 Fast Channels.

The 1904S Peripheral Simultaneity Rules apply.

4.0 EXECUTIVE

As for 1904S, see page 540.3.

5.0 HARDWARE GENERAL DESCRIPTION

5.0.1 For description of 1904S* Mark 1 and 1904S Mark 1, see 1904A General Description page 520.5. For description of 1904S* Mark 2, see 1904S General Description page 540.4.

For description of Main Store, see page 520.10 (Core Store), or page 540.10 (MOS Store).

5.2 Mill Timer

An estimate of clocked time in seconds for 1904S* Mark 1 and 1904S* Mark 2 may be obtained by multiplying the clock pulse count by (to be supplied)

Thus CLOCKED NN X 0.42 ≃pp seconds

5.3 Hesitation Times

To be provided.

6.0 PHYSICAL CHARACTERISTICS

See 1904A or 1904S and Stores as appropriate, pages 520.10 and/or page 540.12.

7.0 FIELD ENHANCEMENTS

For details of fitting F1160/00, F1161/00, F1162/00 or F1163/00 see page 540.16.

For details of fitting F1165/00, F1389/00 or F1900 see page 540.17.

7.1 Store Conversions

For details of Core Store conversions, see page 520.16.

For details of MOS Store conversions, see page 540.17.

7.2 Store Replacement

This involves the removal of the core stores including all core store cabinets and cables and replacing these by the appropriate size of MOS Store including cabinets and cables. Any additional work involved is dependent on the modification level of the particular processor.

8.0 PERFORMANCE (1904S* Mark 1 & 1904S* Mark 2)

8.0.1 All instruction times and work mix times quoted apply to instructions or work mix programs held in even numbered store blocks on systems without Store Extension Units (SEUs) and with standard 14' cables between the Central Processors and Core Stores. The times quoted may be degraded due to the addition of an SEU, the use of longer store cables or for instructions held in odd numbered store blocks by the percentages given below, except where explicitly stated otherwise.

a) Less than 4% if an SEU is fitted.

b) Less than 2% due to the use of 20' store cables.

c) Less than 4% for odd numbered store blocks.

All tolerences, where given, and degradation figures, where applicable, are additive.

8.1 Work Mixes

The times quoted are subject to a machine tolerence of ±5% plus an additional tolerence of +1%-2% due to the method of measurement being dependent on the 50Hz mains frequency at the time the measurements are taken. See also 8.0.1 above.

Post Office Work Unit II (POWU II)

Non Paged System	2.4 milliseconds
Paging Switched OFF	2.9 "
Paging Switched ON	3.3 "

GAMM Mix (with F1160/00 fitted)

Non Paged Machine	10.5 microseconds
Paging Switched OFF	11.5 "
Paging Switched ON	12.5 "

8.2 Fixed Point Instruction Times

8.2.1 The instruction times quoted below are subject to a tolerence of ±10%. The timings may be further degraded as follows:

a) By the figures given in 8.0.1 above.

b) By an additional tolerence of +1%-2% due to the method of measurement depending on the mains frequency at the time the measurements are taken.

All times are applicable to 15 bit and 22 bit address modes of working.

N.B. For modified orders marked * add 0.25 microseconds to times quoted.

Fixed Point Times in microseconds (1904S* Mark 1 & 1904S* Mark 2)

FUNCTION	Non-Paged Machine	Paging OFF	Paging ON
*000	2.21	2.49	2.75
*001	2.21	2.49	2.75
*002	2.21	2.49	2.75
*003	2.21	2.49	2.75
*004	2.21	2.49	2.75
*005	2.21	2.49	2.75
*006	2.21	2.49	2.75
*007	2.21	2.49	2.75
*010	2.28	2.42	2.74
*011	2.66	3.02	3.54
*012	2.28	2.42	2.74
*013	2.66	3.02	3.54
*014	2.28	2.42	2.74
*015	2.66	3.02	3.54
*016	2.28	2.42	2.74
*017	2.66	3.02	3.54

FUNCTION	Non-Paged Machine	Paging OFF	Paging ON
*020	2.21	2.49	2.75
*021	2.21	2.49	2.75
*022	2.21	2.49	2.75
*023	1.23	1.37	1.56
*024	2.21	2.49	2.75
*025	2.21	2.49	2.75
*026	2.21	2.49	2.75
*027	2.21	2.49	2.75
*030	2.66	3.02	3.54
*031	2.66	3.02	3.54
*032	2.66	3.02	3.54
*033	2.66	2.42	2.74
*034	2.66	3.02	3.54
*035	2.66	3.02	3.54
*036	2.66	3.02	3.54
*037	2.66	3.02	3.54
*040	10.30	10.49	10.76
*041	10.30	10.49	10.76
*042	10.30	10.49	10.76
*043	5.11	5.39	5.65
*044	13.30	14.02	14.28
*045	14.90	15.64	15.89
*046	13.70	14.41	14.67
*047	9.54	10.06	10.90
050	1.93	2.07	2.14
052	1.93	2.07	2.14
054	1.93	2.07	2.14
056	1.93	2.07	2.14
060	1.93	2.07	2.14
062	1.93	2.07	2.14
064	1.93	2.07	2.14
066	1.93	2.07	2.14
070	2.23	2.37	2.66
072	2.23	2.37	2.66
074	1.53	1.67	1.74
076	1.53	1.67	1.74
100	1.78	1.92	1.99
101	1.78	1.92	1.99
102	1.78	1.92	1.99
103	1.78	1.92	1.99
104	1.78	1.92	1.99
105	1.78	1.92	1.99
106	1.78	1.92	1.99
107	1.78	1.92	1.99

FUNCTION	Non-Paged Machine	Paging OFF	Paging ON
110	1.48 + 0.3N	1.62 + 0.3N	1.69 + 0.3N
112	1.48 + 0.3N	1.62 + 0.3N	1.69 + 0.3N
114	2.38 + 0.4N	2.52 + 0.4N	2.59 + 0.4N
116	6.76 + 3.66N	7.14 + 4.04N	7.99 + 4.56N
111	2.08 + 0.3N	2.22 + 0.3N	2.29 + 0.3N
113	2.08 + 0.3N	2.22 + 0.3N	2.29 + 0.3N
115	3.98 + 0.4N	4.12 + 0.4N	4.19 + 0.4N
*117	2.86	3.14	3.40
120	1.78	1.92	1.99
121	1.78	1.92	1.99
122	1.78	1.92	1.99
123	1.48	1.62	1.69
124	3.98	4.12	4.19
125	1.78	1.92	1.99
126	5.96 + 1.63N	6.34 + 1.77N	7.14 + 2.11N
127	2.48 + 0.98N	2.62 + 1.12N	2.69 + 1.31N

N = No. of places shifted, moved or normalised.

8.3 Floating Point Instruction Times

8.3.1 The instruction times quoted below apply only to 1904S* Mark 1 and 1904S* Mark 2 systems fitted with F1160/00 Hardware Floating Point Unit.

It is possible for both fixed point and floating point functions to be executed simultaneously. There are up to 4 phases applicable to floating point instructions and only phase 4 is capable of overlap.

8.3.2 In phase 1 the instruction is fetched from store by the central processor; in phase 2 the N address is modified; in phase 3 the central processor loads the operand into the floating point unit (or unloads the operand into store), and in phase 4 the floating point unit executes the instruction. As soon as phases 1, 2 and 3 have been completed the central processor is free to continue with fixed point instructions or to executive phases 1, 2 and 3 of another floating point instruction (there is a buffer available in the floating point unit to queue a second floating point order). If phase 4 of the first instruction is still in progress and a third floating point instruction is encountered it will be executed to the end of phase 2 and the central processor will be held up until phase 4 of the first floating point instruction is completed. Since none of the 076, 136 or 137 instructions involve the floating point unit in any actual calculation, there can be no overlap for any instructions that follows them but if a 076, 136 or 137 instruction follows one of the other floating point orders, then overlap applies in the normal way.

8.3.3 The timings in microseconds for phases 1, 2 and 3 are as follows:

		Non-Paged Machine	Paging OFF	Paging ON
Phase 1	Fetch Instruction	1.23	1.37	1.44
Phase 2	Modification	0.25	0.25	0.25
Phase 3	Load Operand	1.75	2.04	2.42
Phase 3	Unload Operand	2.90	2.90	3.20

An SEU will not degrade the above times by more than:

Phase 1 + 0.03 microseconds
Phase 3 + 0.06 microseconds

For degradation due to odd numbered store modules or longer than 14' store cables see 8.0.1.

All above times are subject to a tolerence of ±10%.

8.3.4 Phase 4 timings are not subject to any degradation due to the use of non-standard length store cables or paging. They are however subject to a machine tolerance of +1%-2% due to mains frequency variation.

Timings in microseconds are as follows:

FUNCTION	130	131	132	133	134	135	136	137
MIN/U	-	2.0	3.0	3.0	10.0	22.5	-	-
MAX/U	-	25.5	9.5	9.5	10.5	25.0	-	-
MIN/N	2.5	-	4.0	4.0	11.0	23.0	-	-
MAX/N	26.0	-	28.0	28.0	47.6	42.5	1.0	1.0

MIN = Minimum calculation (no rounding, correction or alignment required)

MAX = Maximum calculation (rounding, correction and alignment required)

/U = Un-normalised operand (no normalising required)

/N = Normalised operand (normalising required)

8.4 I/O Performance

The figures given below are maximum data transfer rates and are given as general information only. They cannot be used as the basis of checking peripheral simultaneity because this depends on worst case maximum peripheral data transfer rates, crisis time considerations, the effect of PAC transfers on the SHC and other factors beyond the scope of this manual. The actual data transfer rate achieved on any system depends on the peripheral configuration, the connectivity to the system and the program(s).

Maximum I/O Throughput per system:

a) Single PAC with High Speed Channel	3.0 Mch/second
b) Single PAC without High Speed Channel	2.2 Mch/second
c) Dual PAC with 1 or 2 High Speed Channels (1904S* Mark 2 only)	5.0 Mch/second
d) Dual PAC without High Speed Channels (1904S* Mark 2 only)	4.4 Mch/second

Maximum data transfer rate of

a) High Speed Channel	1.5 Mch/second
b) Fast Channel (or PAC Data Buffer) (See Note 1)	380 Kch/second
c) Slow Channel (See Note 2)	
i) Burst Mode (4-Character)	80 Kch/second
ii) Single Character	30 Kch/second

NOTE 1: More than one Fast Channel may be connected to a PAC data buffer therefore the maximum data transfer rate of all Fast Channels sharing one data buffer is 380 Kch/second.

2: The maximum data transfer rate of a Slow Channel is the same as that for the SHC as a whole which is given by:

$$\frac{10^6}{\text{Hesitation Time in microseconds}}$$ (See 5.3)

However, because SHC activity heavily degrades the processor performance and is itself degraded by PAC activity it would not be sensible to allow fast peripherals to be connected via the SHC Slow Channels. The data transfer rates given for Slow Channels are not therefore the maximum imposed by the hardware but are a guide to the practical limits that are imposed. The Simultaneity Rules determine whether any given peripheral may be connected via a Slow Channel or not.

9.0 ORDER VETTING CHECKLIST (Enhancement Orders)

1. Check that the correct system number has been quoted on the order form.

2. If additional peripherals are specified:

   a) Check that they are supported by the Executive used. See Appendix A.

   b) Check peripheral simultaneity and that the correct quantity and types of I/O Channels have been specified. See Appendix B.

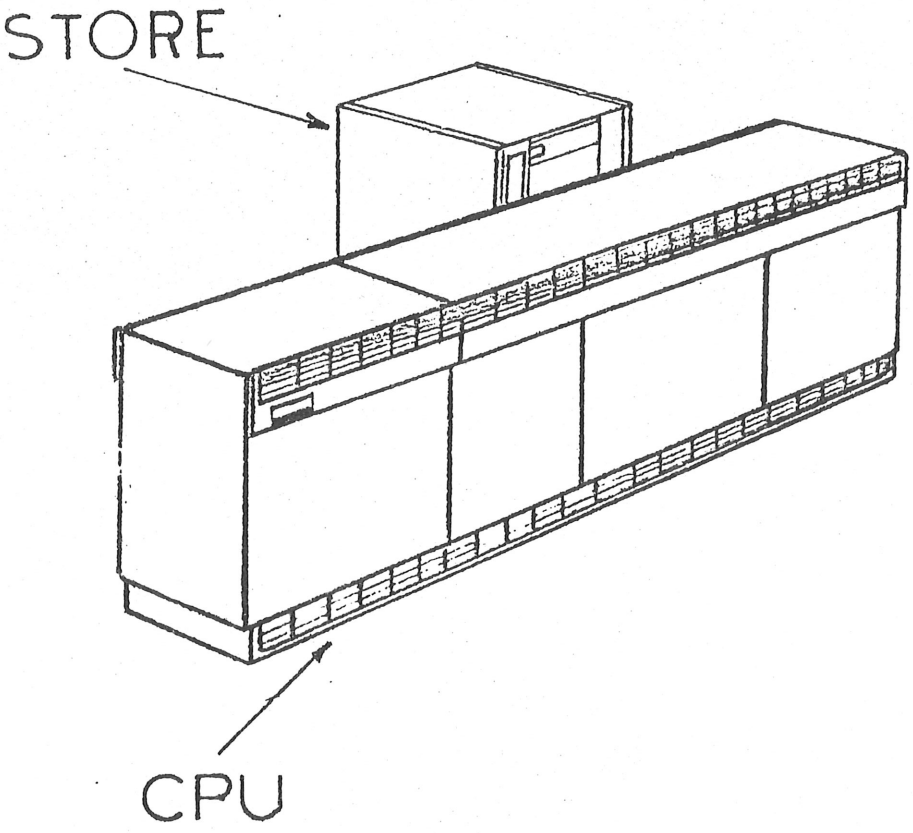
3. If peripheral switches have been specified check that a switching diagram has been attached to the order.

4. If communications equipment is specified check that a diagram of the communications system is included on the Communications Specification Form.

5. See appropriate peripheral ORDER VETTING CHECK LISTS for dependencies, features, etc. applicable to the peripherals or peripheral sub-systems.

6. If peripherals are withdrawn, ensure that the system is still maintainable, i.e. that at least one CR or PTR and one LP remain. Check also that the peripheral requirements of the Executive and/or Operating System are met. See Section 2.

1904S Processor



1.0 INTRODUCTION

1.0.1 The 1904S is a medium to high-power general-purpose processor, designed to process both commercial and scientific applications. Systems may be configured from the components listed in 2.1 and 2.2 below and the peripherals listed in Appendix A under the type of Executive used. All connected peripherals must be able to run simultaneously and appropriate I/O Channels must be provided for them.

NOTE: This entry describes a full specification 1904S system; other 1904S systems, derived by enhancement from 1904A, may have reduced performance and facilities depending on the Machine Number of the converted 1904A and whether or not the enhancement included replacement of the Core Store by MOS Store. For details of these systems see Reduced Facility 1904S Systems, page 530.1.

1.1 Summary of Characteristics

Order Code Level	C
Main Store Cycle Time	500 Nanoseconds
POWU II	2.3 Milliseconds
GAMM Mix (with H/W Option F1160/00)	10.5 Microseconds
Total I/O throughput: 2 x PAC	5.0 Mch/second
1 x PAC	3.0 Mch/second
PAC less High Speed Channel	2.20 Mch/second
Main Store Size (MOS Store)	64K words to 256K words

2.0 TYPE NUMBERS & CONSTITUENT ITEMS

2.1 Standard Components

Type Number	Description
2046/00	Central Processor comprising the following: Central Processor Unit (CPU) including: (a) 8 Hardware Accumulators (b) Real Time Clock (c) Mill Timer (d) Slow Hesitation Control (SHC) with 6 Slow Channels Peripheral Autonomous Control (PAC) with 4 Fast Channels. DC Power Supply Units Console Typewriter Desk with Console Typewriter and and operator's controls for loading and running the system. Extension Console Typewriter Desk with Console Typewriter and operator's controls permitting isolation of faulty store modules and switching control between the two Console Typewriters.
2046/05	96K words of Main Store)
2046/06	128K words of Main Store) Select appropriate size
2046/08	192K words of Main Store*)
2046/09	256K words of Main Store*)
	*Includes a Store Extension Unit

2.2 Optional Hardware Features

The following items may be supplied either as part of the original order or as field fitments:

Type Number	Description
F1160/00	Floating Point Unit
F1161/00	Fast Peripheral Channel (maximum 8 on Basic PAC, 6 on 2nd PAC)
F1162/00	High Speed Channel (maximum 1 per PAC)
F1163/00	Group of 6 Slow Channels (maximum 2)
F1165/00*	Paging Feature
F1389/00*	2nd Peripheral Autonomous Control (Channels must be specified separately as required)
F1900/00	Main Store Switching Feature (permits store switching between two adjacent 1904S systems). Comprises additional store cables and SEU's as required; see 5.3.2 for ordering procedure.

*These features are mutually exclusive.

2.3 Conversions

Type Number	Description
C1181/00	Conversion of 2046/05 to 2046/06
C1182/00	Conversion of 2046/06 to 2046/08
C1183/00	Conversion of 2046/08 to 2046/09

2.4 Basic Accessories

The items listed below are provided automatically, free of charge, with each 1904S Central Processor.

Description	Qty.
Console Chair	1
Console Typewriter Stationery ($8\frac{1}{2}$" x 200" roll, 2-part)	1 each per 2 Console
Ribbons	2 Typewriter

Additional supplies may be obtained from Dataset and are chargeable to the customer.

3.0 CONNECTIVITY

3.0.1 There are three aspects of connectivity relating to the attachment of 1900 Series peripherals to 1904S that must be satisified:

a) All connected peripherals must be supported by the Executive(s) to be used with the system.
b) The correct type of I/O Channel must be provided for the connection of each peripheral.
c) The total peripheral configuration must be able to run with simultaneity.

To satisfy requirement a) it is necessary to determine the type of Executive(s) to beused by reference to 4.0 below, then to refer to the Approved Central Processor/Peripheral Connections table for that Executive(s), given in Appendix A, to determine whether any given peripheral(s) is supported by that Executive(s). To satisfy requirements b) and c) use the information given in 3.1 below in conjunction with the 1903T, 1904A, 1904S Peripheral Simultaneity Rules given in Appendix B.

3.1 I/O Channels & Peripheral Simultaneity

3.1.1 The 1903T, 1904A, 1904S Peripheral Simultaneity Rules determine the types of I/O channels that can be used with different types of peripherals on these processors and give the loading figures (IMTAC Value or α - Factor) applicable to each peripheral. The maximum number of I/O channels of each type available, the maximum number of data buffers in PAC and the maximum peripheral loading values permited on 1904S are as follows:

Max. number of High Speed Channels	2	(1 per PAC optional)
Max. number of Fast Channels:		
a) on basic PAC	12	(basic 4+8 optional)
b) on 2nd PAC	6	(optional)
Max. number of Slow Channels	18	(basic 6+2 groups of 6 optional)
Max. number of Data Buffers on each PAC	6	(supplied as required)
Max. IMTAC Value allowed on processor	1250	
Max. IMTAC Value allowed on each PAC	750	
Max. IMTAC Value per Data Buffer	95	
Max. IMTAC Value per Fast Channels on each PAC:		
(a) If no High Speed Channel on PAC	550	
(b) If High Speed Channel on PAC	750	- IMTAC Value of the peripheral on High Speed Channel or 550 whichever is less.

Maximum α - Factor allowed on SHC is given by:

$$725 - 0.15I$$

(where I = the total IMTAC Value on the processor, see Appendix B, 3.0.6).

4.0 EXECUTIVE

4.0.1 The following Executives may be used with a 1904S:

Unpaged System or paging switched OFF	Paged system with paging switched ON
E6RM	EWG4 (with GEORGE 4)
EWG3 (with GEORGE 3)	

For further details of Executive, including compile-time options, store occupancy and peripheral requirements see Section 2.

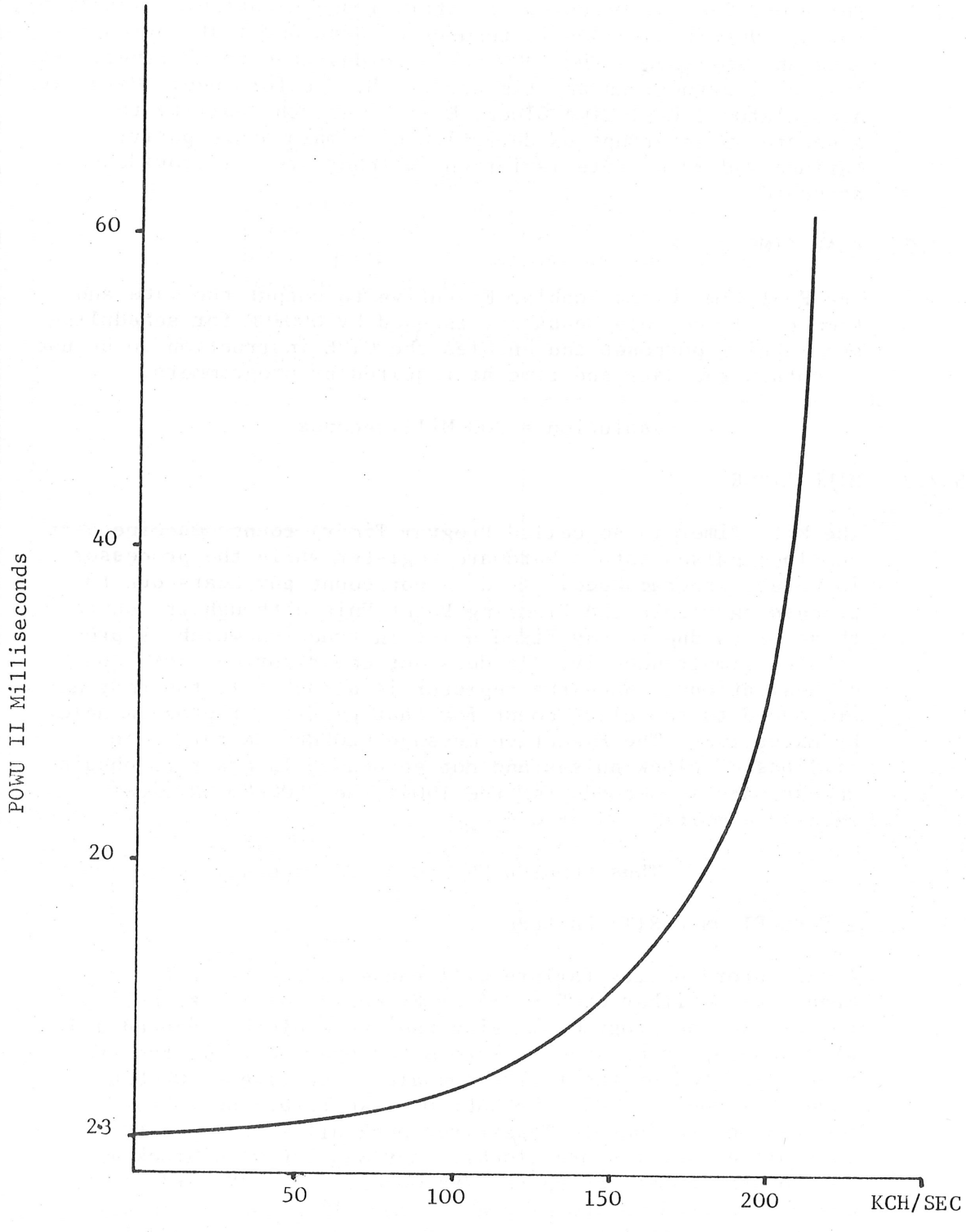


Figure 2 1904S Performance Degradation Due To SHC Activity

(a) the number of outstanding units of transfer,
(b) the absolute address of the next unit and
(c) the style of transfer

are held in control words, which are read and updated once for each unit of data written to or read from main store. The four characters of a burst from a burst-mode peripheral are assembled into one word before being presented to main store.

5.2.6 SLOW HESITATION CONTROL

The SHC is an integral part of the CPU and the CPU mill is used to update the control words which are held in main store. The processor's B-register is used to assemble 4-characters serially into one word during a burst-mode transfer. For these reasons a data transfer via SHC and instruction processing cannot go on simultaneously and a peripheral request for data transfer must wait until the processor's mill and registers are in a condition to deal with the request. After such a delay the processing of instructions will hesitate for the duration of the transfer. The maximum CPU delay and SHC hesitation times, assuming no interference from PAC which has priority for main store access, are given below:

Type of Hesitation	Nominal Time in microseconds Input	Output
Single Character Single Channel	Individual times to be supplied. Meanwhile assume time spent in each SHC hesitation routine = 18.4 microseconds	
Four Character Single Channel		
Single Character Multi Channel		
Four Character Multi Channel		
Control Word Recharge		
Scatter read-gather write*		
Maximum CPU delay		

* only when the paging feature is used and when a page boundary is crossed.

The effect of data transfers via the SHC on processor performance is indicated in Figure 2.

5.2.7 PERIPHERAL AUTONOMOUS CONTROL

Two PAC's may be fitted to the 1904S. Each is an autonomous unit comprising a main control and mill, control word buffers and data buffers. The first PAC is standard and will have direct access to store except when a 2nd PAC (F1389/00) is fitted. In the latter case both PAC's are connected to store via a branching unit which is supplied with the 2nd PAC. The logical structure of a PAC is shown in Figure 4 below. The control word buffers and data buffers are supplied as required; one pair of control word buffers per channel connected, High Speed data buffers and up to 6 Fast data buffers depending on the number and type of peripherals connected. Since PAC has priority for store access, the processor will be forced to hesitate when a clash occurs, consequently instruction processing may be held up or SHC hesitations may be interrupted.

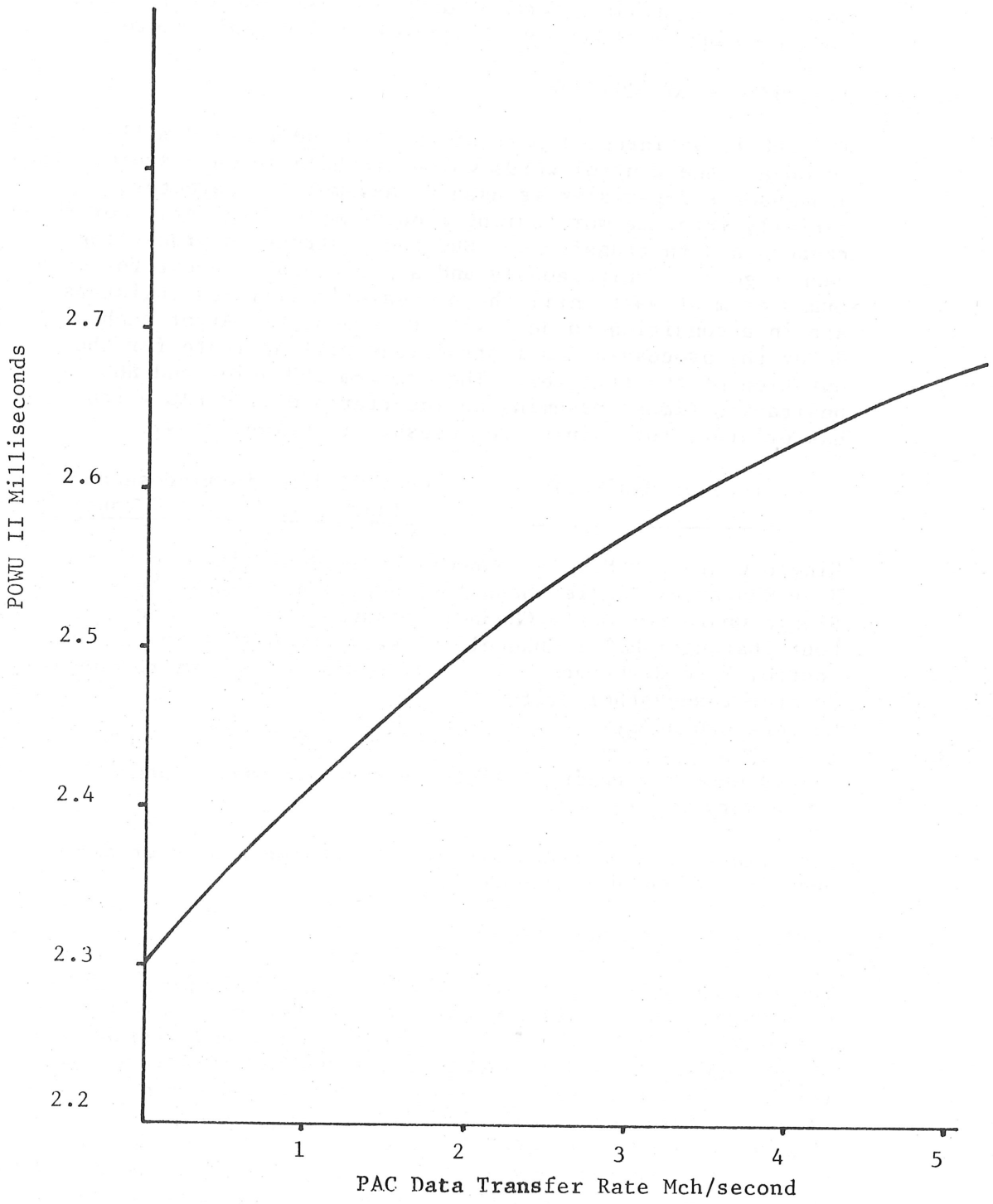
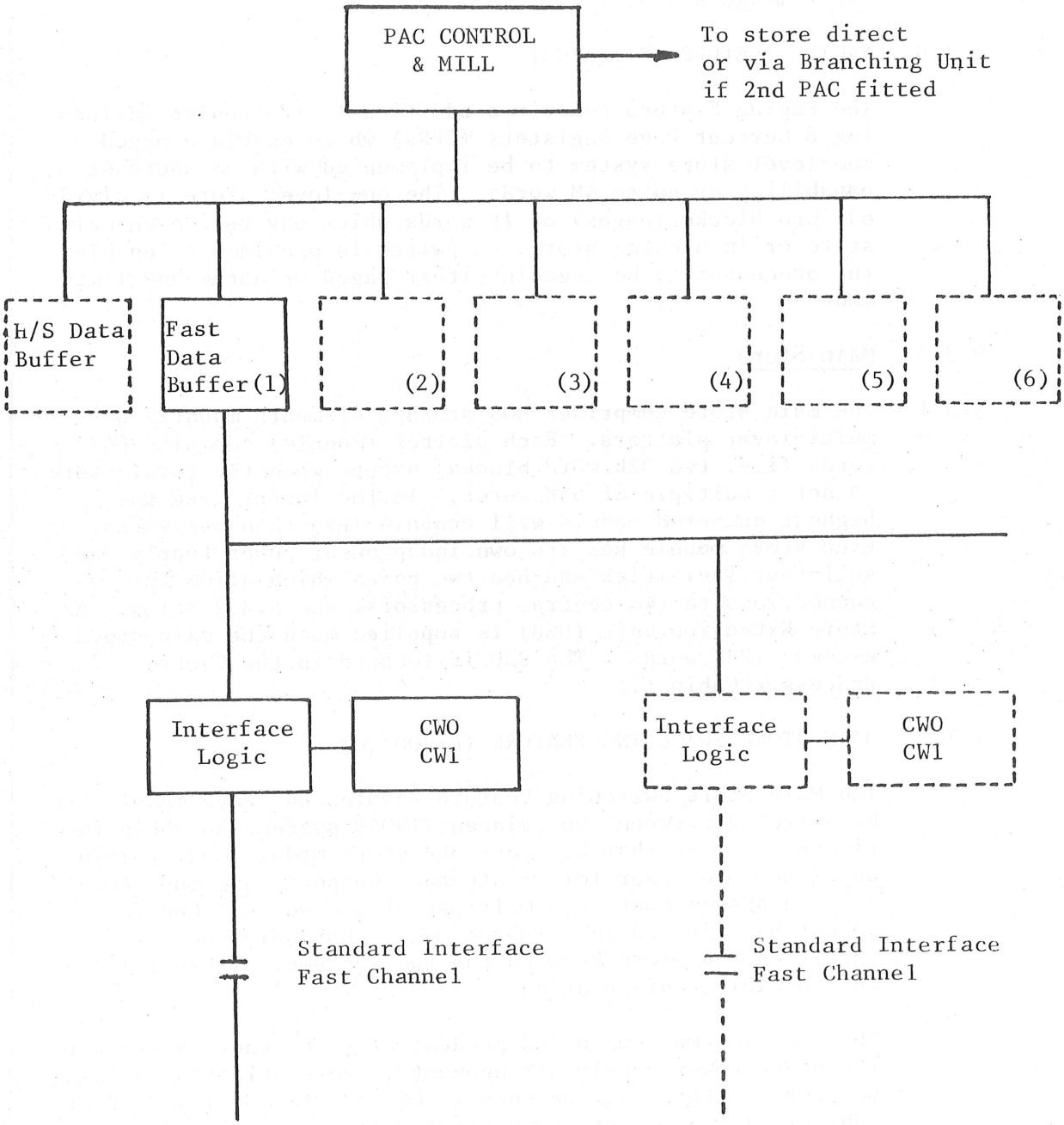


Figure 3 1904S Performance Degradation Due To PAC Activity

However, since many operations in the central processor do not involve the store, the average delay experienced by the processor will be significantly less than the maximum and is taken into account in calculating the degradation in processor performance due to PAC activity illustrated in Figure 3. The simultaneity rules take account of the effect of PAC on SHC timings.



Connections to 4-character peripherals

Figure 4 Logical Structure of 1904S PAC

5.2.8 FLOATING POINT UNIT (F1160/00)

The Floating Point Unit comprises additional electronics including a hardware floating point accumulator. It operates autonomously with the CPU during the execution phase of floating point instructions and provides results identical to those obtained with the Floating Point Units on 1907, 1905F, 1903T and 1904A. For list of instructions and timings see 8.3.

5.2.9 PAGING FEATURE (F1165/00)

The Paging Feature comprises additional electronics including 8 Current Page Registers (CPRs) which enable a paged one-level store system to be implemented with an addressing capability of up to 4M words. The one-level store is divided into blocks (pages) of 1K words which may reside in main store or in backing store. A switch is provided to enable the processor to be used in either paged or datum and limit mode.

5.3 Main Store

5.3.1 The main store comprises MOS storage elements mounted on multi-layer platters. Each platter (module) contains 64K words (i.e. two 32K word blocks) except when the total store is not a multiple of 64K words. In the latter case the highest numbered module will contain less than 64K words. Each store module has its own independent power supply and self-test facilities and has two ports which allow for connections to two central processors, see 5.3.2 below. A Store Extension Unit (SEU) is supplied when the main store exceeds 128K words. The SEU is located in the Central Processor Cabinet.

5.3.2 MAIN STORE SWITCHING FEATURE (F1900/00)

The Main Store Switching Feature enables 64K word modules to be switched between two adjacent 1904S systems as shown in Figure 5. Note that at least one store module must remain on either processor for maintenance purposes and the store on each system must be a multiple of 64K words. Modules cannot be switched in a random manner but only such as to partition the store between the two systems. Table 1 lists the possible configurations.

The two systems remain independent of each other except for the store power supply arrangements. Any cabinet(s) holding switchable store must be powered ON and OFF locally at that cabinet(s). At least one cabinet will be associated with each processor and an over-temperature condition occurring in a store cabinet will power OFF that cabinet and cause an interrupt only to the processor associated with that cabinet. The other processor will not receive an interrupt even though part of the store housed in that cabinet is switched to it.

Store cabinets can hold up to 128K words each and are supplied

as required. Note that two 192K systems can be accommodated in 3 store cabinets and normally only 3 cabinets will be supplied. The maximum store that can be connected to any processor is 256K words.

Table 1 Possible Store Configurations

Store specified on each system	Possible Configurations		Number of store cabinets
	Processor A	Processor B	
128K 128K	64K 128K 192K	192K 128K 64K	2
128K 192K	64K 128K 192K 256K	256K 192K 128K 64K	3
128K) 256K) Fig.5	128K 192K 256K	256K 192K 128K	3
192K 256K	192K 256K	256K 192K	4

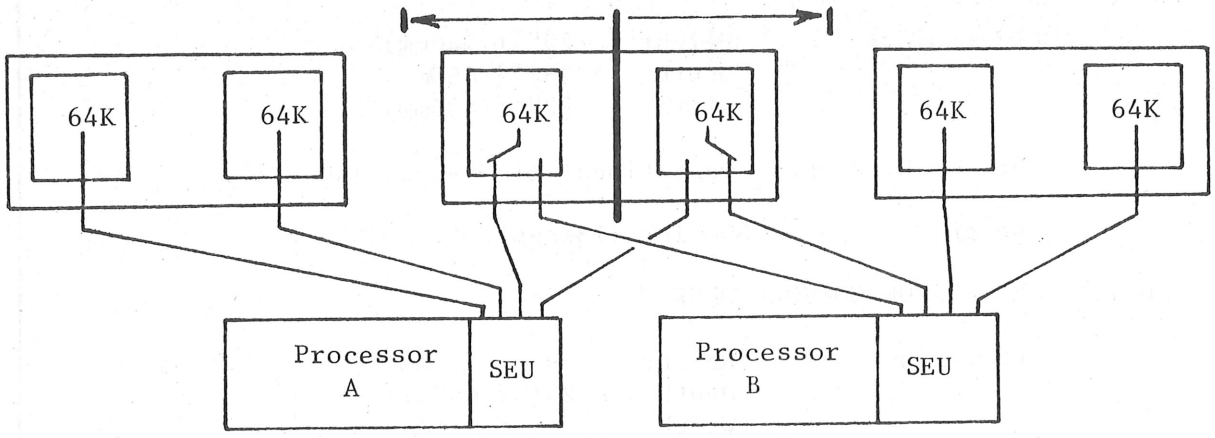


Figure 5 Store Switching Between Two Adjacent 1904S Processors (128K, 256K)

Note: Ordering Procedure
F1900/00 may be ordered against either one of the two systems. Main store must be ordered on both systems, i.e. it canot all be specified against one system only. When F1900 is ordered, the number of store modules to be switched and the other system number must be stated so that the correct number of cables and SEUs can be be supplied. See also Table 1 and 5.3.2 above.

6.0 PHYSICAL CHARACTERISTICS

6.1 Dimensions & Weight

6.1.1 CENTRAL PROCESSOR

Dimensions	Height	55" (1400mm)
	Depth	28½"(720mm)
	Length	140" (3556mm)
Access Clearance	Front	54" (1370mm)
	Rear	54" (1370mm)
	Left	-
	Right	36" (910mm)
Weight		1500 lbs (681Kgs).

6.1.2 MAIN STORE CABINET

Dimensions	Height	67" (1700mm)
	Depth	29½"(749mm)
	Length	27" (689mm)
Access Clearance	Front	47" (1200mm)
	Rear	47" (1200mm)
	Left	12" (305mm)
	Right	12" (305mm)
Weight		605 lbs (270Kgs).

6.1.3 CONSOLE TYPEWRITER DESK

Dimensions	Height	29" (740mm)
	Depth	25½"(650mm)
	Width	72" (1830mm)
Access Clearance		Operational clearances (see 6.5)
Weight		300 lbs (136Kgs).

6.1.4 EXTENSION CONSOLE DESK

Dimensions	Height	29" (740mm)
	Depth	25½"(650mm)
	Width	36" (914mm)
Access Clearance		Operationa clearances (see 6.5)
Weight		200 lbs (91Kgs).

6.2 Mains Supply

A Motor Alternator is mandatory. This may be 1986/02 (45KVA), 1986/07 (65KVA) or 1986/08 (100 KVA) depending on the total system requirements.

In any case the mains supply required will be phase 50Hz.

6.3 Power Requirements & Heat Dissipation

6.3.1 Power Required

Central Processor		4.1 KVA
Main Store	96K	2.0 KVA
	128K	2.0 KVA
	192K	3.2 KVA
	256K	4.0 KVA
Consoles		0.4 KVA

6.3.2 Heat dissipation

Central Processor		3.0 KW
Main Store	96K	1.6 KW
	128K	1.6 KW
	192K	2.545 KW
	256K	3.2 KW
T/W Consoles		0.3 KW

6.4 Environment

Temperature range	$10^{o}C$ - $35^{o}C$
Relative Humidity	20% - 80%
Air Cleanliness	Air filtering not required under normal office conditions.

6.5 Site Layout

6.5.1 The possible relative positions of the Central Processor, Main Store and Console Typewriter Desk are determined by the physical space available, cable lengths, access clearance required and the operational requirements of the system as a whole. CED Environmental Engineering must be consulted regarding all site layouts.and can advise on the best layout taking into account all the relative factors.

The details given below are for guidance only.

6.5.2 CABLE LENGTHS

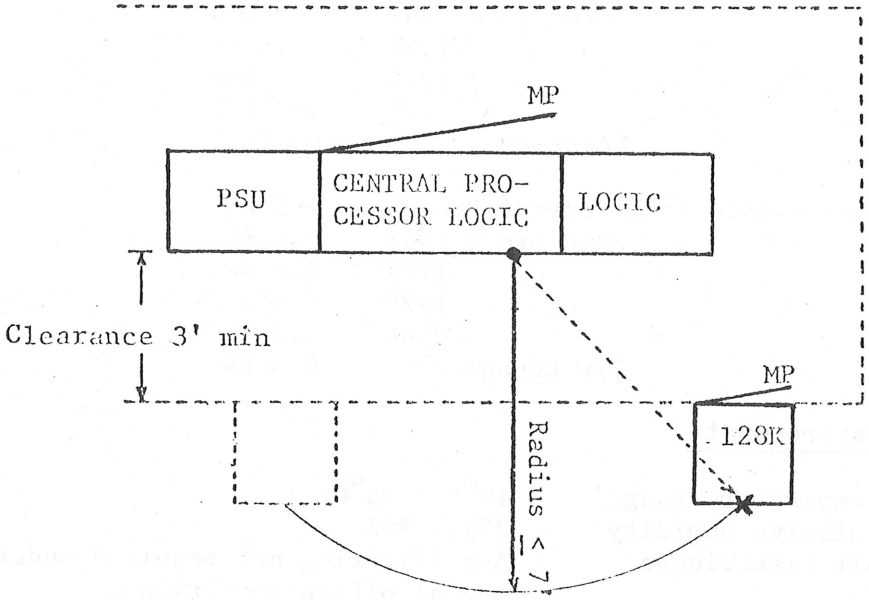
	Standard	Other*
Processor - Store	10' (3.05m)	14' (4.26M) 20' (6.1M)
Processor - C/TW Desk	45'(13.73m)	Up to 100' (30.5M)
C/TW Desk - Extension Desk	The normal length cable supplied allows the Extension Desk to be positioned immediately to the right of the Console Desk. For a remote position, cables of length 20' (6.1M) are available allowing the Extension Desk to have a physical separation of 15' (5M) to the right or 10' (3M) to the left of the Console Desk.	

*Where non-standard cables are required they will be ordered from Production by CED. The use of other than the standard 10' Processor-Store cables will degrade the system performance, see 8.0.1 for details.

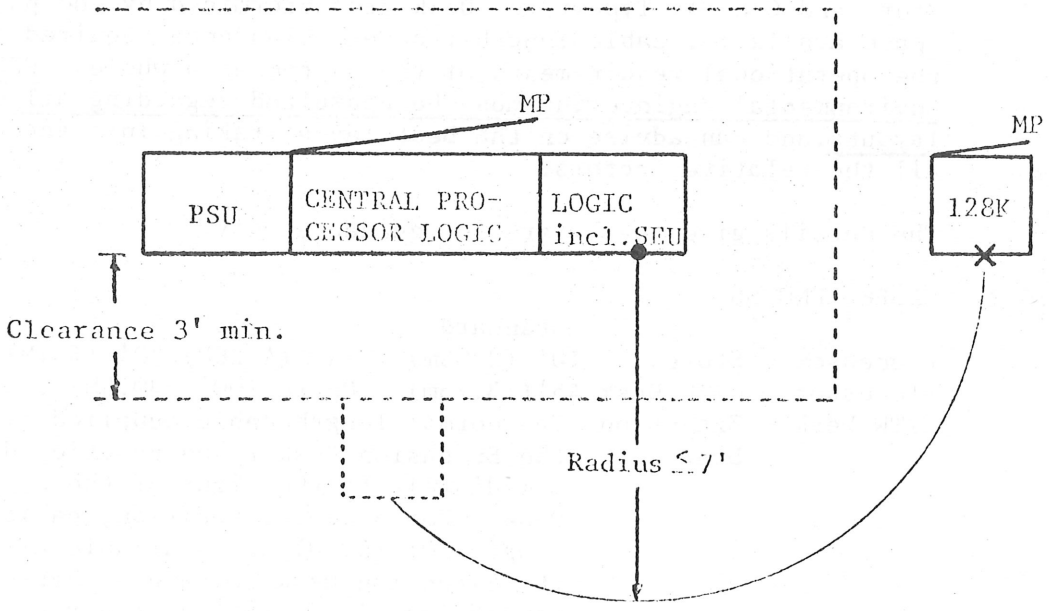
6.5.3 STANDARD LAYOUTS

When standard 10' cables are used processors and stores must be located as shown in Figure 6. Store cabinets should be positioned so that the monitor panel is visible to an Engineer stood at

the processor's monitor panel. When Store Switching (F1900/00) is used the two processors systems must be positioned as shown in Figure 7.



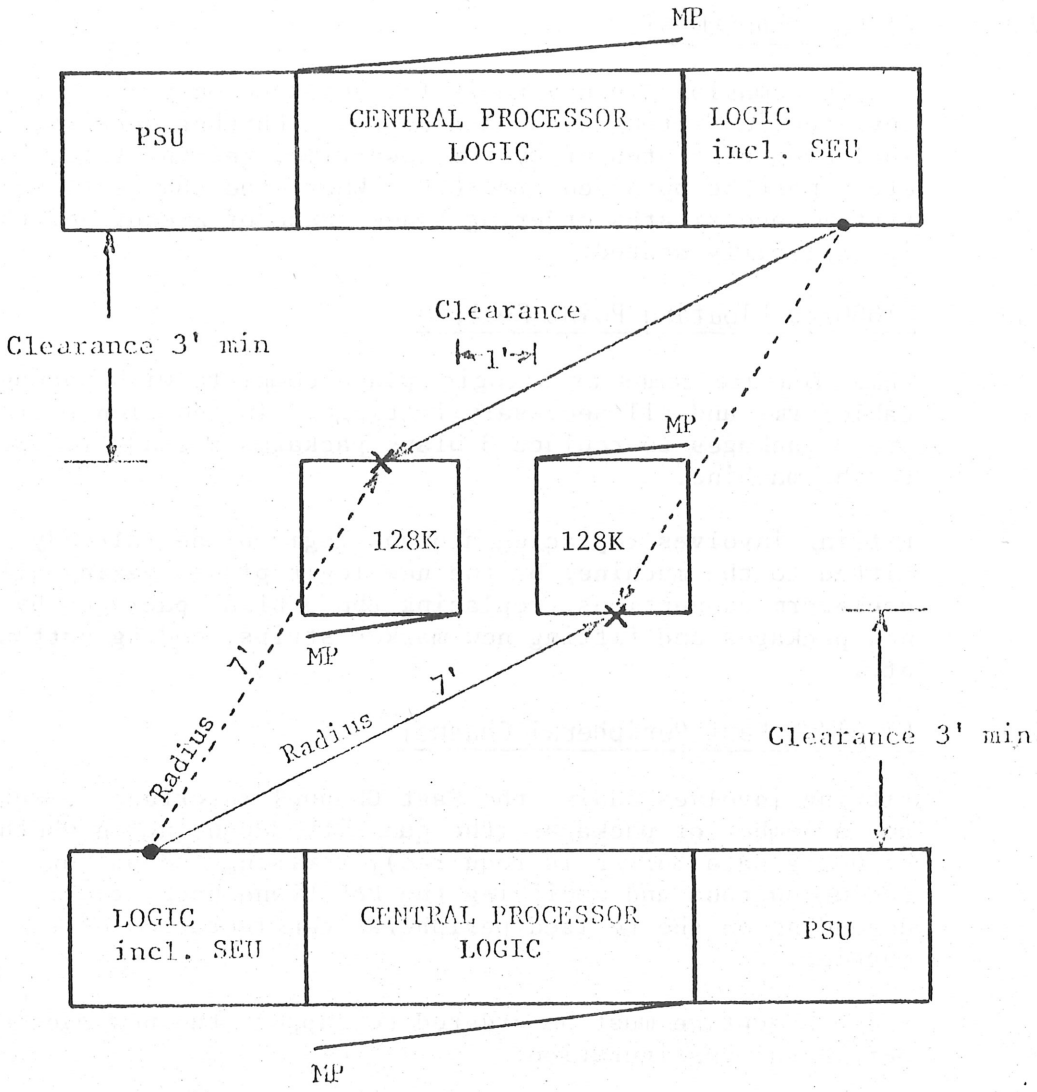
Processor + up to 128K words



Processor + Greater Than 128K words

PSU = Processor Power Supply Units
• = Processor cable entry
X = Store cable entry
MP = Monitor Panel

Figure 6 1904S Processor/Store Standard Site Layouts



PSU = Processor Power Supply Units
● = Processor cable entry
X = Store cable entry
MP = Monitor Panel

Figure 7 Standard 1904S Processor/Store Site Layout With Store Switching (F1900/00) and 2 Store Cabinets

(For layout details of 3 or 4 Store Cabinet systems contact CED Environmental Engineering)

7.0 FIELD ENHANCEMENTS

The information given here is for guidance only on what is involved in fitting each enhancement. Further details, including estimates of system down-time, testing time, etc. must be obtained from CED. Where the change to the system necessitates ordering a new issue of Executive, this is explicitly stated.

7.1 F1600/00 Floating Point Feature

This feature comes as a logic plane complete with packages, cableforms and all necessary fittings. In addition there are 3 packages to replace 3 blank packages already fitted to the machine.

Fitting involves replacing a blank logic plane (already fitted to the machine) by the new logic plane, making all cableform connections, replacing the 3 blank packages by new packages and fitting new marker strips, coding buttons, etc.

7.2 F1161/00 Fast Peripheral Channel

Fitting involves adding the Fast Channel interface socket and a number of packages (the quantity depending on whether or not a Data Buffer is required), revising the package coding buttons and modifying the PAC Plane backwiring, depending on the revised peripheral configuration of the machine.

A new Executive must be ordered to support the new machine peripheral configuration.

7.3 F1162/00 High Speed Peripheral Channel

Fitting involves adding the High Speed Channel interface socket and making connections to the PAC Plane, replacing 7 packages, adding 2 additional packages and revising the package coding buttons.

A new Executive must be ordered to support the new machine peripheral configuration.

7.4 F1163/00 Group of 6 Slow Channels

Fitting involves adding the Slow Channel interface sockets and packages and connecting the channels to the corresponding channel positions on the Distribute Plane.

A new Executive must be ordered to support the new machine peripheral configuration.

7.5 F1165/00 Paging Feature

This feature comes as a logic plane assembly complete with packages, cableforms and all necessary fittings and an Engineers Control Panel and monitor panel.

Fitting involves replacing a blank logic plane (already fitted to the machine) by the new logic plane, fitting the Engineers Control Panel and monitor lamp panel, making the cableform connections and replacing blank packages in the Distributer Plane by new packages.

Order Executive EWG4 and GEORGE 4.

7.6 F1900/00 Main Store Switching Feature

Fitting involves connecting the store modules, to be switched, to the processor(s) via store interface cableforms and fitting SEU's if required.

7.7 C1181/00 Conversion of 2046/05 to 2046/06

Fit 32K Store Macro Block to store platter and revise coding buttons.

7.8 C1182/00 Conversion of 2046/06 to 2046/08

This conversion involves adding a 2nd Store Cabinet with 64K of store, linking the stores via cableforms and modifying the Distributer by changing and adding packages and revising the appropriate coding buttons.

7.9 C1183/00 Conversion of 2046/08 to 2046/09

Assemble and mount additional 64K platter in 2nd Store Cabinet. Make all cableform connections and replace a package in the CPU.

FUNCTION CODE	INSTRUCTION TIME IN MICROSECONDS		
	Non-paged Machine	Paging OFF	Paging ON
070-071			
Compact	2.13	2.27	2.58
Rel.	2.73	2.87	3.18
Repl.	3.66	3.94	4.48
072-073	2.13	2.27	2.58
074-075			
No jump	1.43	1.57	1.68
Compact	1.53	1.67	1.98
Rel.	2.13	2.27	2.58
Repl.	2.76	3.04	3.56
076-077	(Assuming Floating Point Unit Isn't Busy)		
No jump	1.53	1.67	1.78
Compact	1.53	1.67	1.98
Rel.	2.33	2.47	2.78
Repl.	2.96	3.24	3.76
100 ($\overline{CY}$)	1.38	1.52	1.63
100 (CY)	1.68	1.82	1.93
101-107	1.68	1.82	1.93
110	1.38+0.3N	1.52+0.3N	1.63+0.3N
111	1.98+0.3N	2.12+0.3N	2.23+0.3N
112(C/L)	1.38+0.3N	1.52+0.3N	1.63+0.3N
112(A/S)	1.68+0.3N	1.82+0.3N	1.93+0.3N
113	1.98+0.3N	2.12+0.3N	2.23+0.3N
114	2.28+0.4N	2.42+0.4N	2.53+0.4N
115	3.88+0.4N	4.02+0.4N	4.13+0.4N
116	6.59+3.55N	6.59+3.97N	7.54+4.59N
117	2.36 - 2.71	2.64 - 2.99	2.96 - 3.31
120-122	1.68	1.82	1.93
123	1.38	1.52	1.63
124	3.88	4.02	4.13
125	1.68	1.82	1.93
126	5.79+1.42N	6.21+1.70N	6.74+2.11N
127	2.38+0.93N	2.52+1.07N	2.63+1.28N

N = Number of places shifted, moved or normalised.

8.3 Floating Point Instruction Times

8.3.1 The instruction times quoted below apply only to 1904S systems fitted with the F1160/00 Hardware Floating Point Unit. It is possible for both fixed point and floating point functions to be executed simultaneously. There are up to 4 phases applicable to floating point instructions and only phase 4 is capable of overlap.

8.3.2 In phase 1 the instruction is fetched from store by the central processor; in phase 2 the N address is modified; in phase 3 the central processor loads the operand into the floating point unit (or unloads the operand into

store), and in phase 4 the floating point unit executes the instruction. As soon as phases 1, 2 and 3 have been completed the central processor is free to continue with fixed point instructions or to execute phases 1, 2 and 3 of another floating point instruction (there is a buffer available in the floating point unit to queue a second floating point order). If phase 4 of the first instruction is still in progress and a third floating point instruction is encountered it will be executed to the end of phase 2 and the central processor will be held up until phase 4 of the first floating point instruction is completed. Since none of the 076, 136 or 137 instructions involve the floating point unit in any actual calculation, there can be no overlap for any instructions that follows them but if a 076, 136 or 137 instruction follows one of the other floating point orders, then overlap applies in the normal way.

8.3.3 The timings in microseconds for phases 1, 2 and 3 are as follows:

	Basic 1904S	Paging OFF	Paging ON
Phase 1 Fetch Instruction	1.23	1.37	1.44
Phase 2 Modification	0.25	0.25	0.25
Phase Load Operand	1.74	2.03	2.41
Phase 3 Unload Operand	2.42	2.42	2.91

An SEU will not degrade the above times by more than:

Phase 1 +0.03 microseconds
Phase 3 +0.06 microseconds

For degradation due to store refresh or the use of longer than the standard 10' cables see 8.0.1.

All above times are subject to a tolerence of ±10%.

8.3.4 Phase 4 timings are not subject to any degradation due to store refresh or the use of non-standard length store cables or paging. They are however subject to a machine tolerance of ±5% plus an additional tolerance of +1% -2% due to mains frequency variation.

Timings in microseconds are as follows:-

FUNCTION	130	131	132	133	134	135	136	147
MIN/U	-	2.0	3.0	3.0	10.0	22.5	-	-
MAX/U	-	25.5	9.5	9.5	10.5	25.0	-	-
MIN/N	2.5	-	4.0	4.0	11.0	23.0	-	-
MAX/N	26.0	-	28.0	28.0	47.5	42.5	1.0	1.0

MIN = Minimum calculation (no rounding, correction or alignment required)
MAX = Maximum calculation (rounding, correction and alignment required)
/U = Un-normalised operand (no normalising required)
/N = Normalised operand (normalising required).

8.4 I/O Performance

The figures given below are maximum data transfer rates and are given as general information only. They cannot be used as the basis of checking peripheral simultaneity because this depends on worst case maximum peripheral data transfer rates, crisis time considerations, the effect of PAC transfers on the SHC and other factors beyond the scope of this manual. The actual data transfer rate achieved on any system depends on the peripheral configuration, the connectivity to the system and the program(s).

Maximum I/O Throughput per system.

a) With 2 PAC's and 1 or 2 High Speed Channels	5.0 Mch/second
b) With 2 PAC's without High Speed Channels	4.4 Mch/second

Maximum data transfer rate of:

a) PAC with High Speed Channel	3.0 Mch/second
b) PAC without High Speed Channel	2.2 Mch/second
c) High Speed Channel	1.5 Mch/second
d) Fast Channel (or PAC Data Buffer) (see Note 1)	380 Kch/second
e) Slow Channel (see Note 2)	
i) Burst Mode	80 Kch/second
ii) Single Character	30 Kch/second

NOTE 1: More than one Fast Channel may be connected to a PAC data buffer therefore the maximum data transfer rate of all Fast Channels sharing one data buffer is 380 Kch/second.

2: The maximum data transfer rate of a Slow Channel is the same as that for the SHC as a whole which is given by:

$$\frac{10^6}{\text{Hesitation Time in microseconds (See 5.2.6)}}$$

However, because SHC activity heavily degrades the processor performance and is itself degraded by PAC activity it would not be sensible to allow fast peripherals to be connected via the SHC Slow Channels. The data transfer rates given for Slow Channels are not therefore the maximum imposed by the hardware but are a guide to the practical limits that are imposed. The Simultaneity Rules determine whether any given peripheral may be connected via a Slow Channel or not.

9.0 ORDER VETTING CHECKLIST

NEW SYSTEM ORDERS

1. Check that the configuration includes all mandatory peripherals required for maintenance purposes and by Executive and/or Operating System. See 9.1 and Section 2.

2. Check that the correct type of Motor Alternator has been specified. See 6.2.

ENHANCEMENT ORDERS

3. Check that the correct system number has been quoted.

ALL ORDERS

4. Check that all peripherals specified are supported by the Executive to be used on the system. See Appendix A.

5. Check peripheral simultaneity and that the correct quantity and types of I/O channels have been specified for the connection of all peripherals. See 3.1 and Appendix B.

6. Where peripheral switches have been specified check that a switching diagram has been included.

7. When peripherals have been retained from some earlier system or from other sources check that these are listed on the specification form.

8. Check that a diagram of all communications configurations is included on the Communications Specification form.

9. See appropriate peripheral ORDER VETTING CHECKLISTS for dependencies, features etc. applicable to the peripherals or peripheral sub-systems.

9.1 Mandatory Peripherals Required For Maintenance Purposes

It must be possible to have at least one suitable input device and one suitable output device connected to a system for maintenance purposes. Either these must be permanently connected to the processor or it must be possible to switch them to the processor by means of Standard Interface Switching Units.
The only input devices suitable are either:

a) An 80 column card reader - with or without Card Image
or
b) A paper tape reader capable of handling ISO 8 channel tape.

The only output devices suitable are either:

a) A line printer with 96 or more print positions, buffered or unbuffered and connected to either PAC or to SHC.
or
b) A paper tape punch, provided there is on the customer's

premises an off-line printer which can accept the paper tape produced by this punch.