1906A Processor

1.0 INTRODUCTION

1.0.1 The 1906A is a large-scale, general purpose processor designed to process both commercial and scientific applications. Its performance is achieved through the use of Emitter Coupled Logic (ECL) technology, instruction pipelining and 2-word wide interleaved store. Data transfers are handled by autonomous Peripheral Processing Unit (PPU). Paging and floating point hardware are optional.

1.0.2 There are two versions of 1906A:-

a) Early systems up to system number 14 which have the type number 2080.

b) Systems numbered 15 onwards which have the type number 2082. These have a revised cabinet layout and modified Peripheral Processing Unit similar to 1906S and giving a higher total data transfer capability.

1.0.3 Systems may be configured from the items listed in 2.1 and 2.2 below and the peripherals listed in Appendix A. All connected peripherals must be able to run simultaneously and appropriate Standard Interfaces must be provided for them.

1.1 Summary of Characteristics

Order Code Level	C
Main Store Cycle time	750 Nanoseconds
Main Store Size	128K words to 512K words (Core Store)
POWU II (4-way interleaved store)	0.93 Milliseconds
GRAM Mix (with H/W option F1148/00)	
a) Normal precision	3.0 Microseconds
b) Extended precision	5.0 Microseconds
Total I/O throughput capability	
a) 2080 version	5.0 M ch./second
b) 2082 version	6.5 M ch./second

2.0 TYPE NUMBERS & CONSTITUENT ITEMS

2.1 Standard Components

Type Number	Description
2080/00	1906A Central Processor comprising the following: a) Central Processor Unit (CPU) including: i) Hardware Accumulators ii) Real Time Clock iii) Instruction/Operand Counter b) Peripheral Processing Unit (PPU) including: i) 4 Fast Peripheral Standard Interfaces ii) 10 Slow Peripheral Standard Interfaces c) DC Power Supply Units and Cooling Units d) Console Typewriter Desk with Console Typewriter. e) Spare Console Typewriter

Type Number	Description	
2082/00	1906A Central Processor. As 2080/00 but with revised cabinet layout and higher throughput PPU.	
2080/02	128K words 750 nsec Core Store	Size Optional
2080/03	192K words 750 nsec Core Store	
2080/04	256K words 750 nsec Core Store	
2080/05	384K words 750 nsec Core Store	
2080/06	512K words 750 nsec Core Store	

2.2 Optional Hardware Features

2.2.1 2080 OPTIONS

Type Number	Description
F1148/00	Extended Precision Floating Point Unit
F1149/00	Paging
F1184/00	1st Slow Interface Enhancement (Block of 6)
F1185/00	2nd Slow Interface Enhancement (Block of 8)
F1186/00	3rd Slow Interface Enhancement (Block of 6)
F1187/00	1st Fast Interface Enhancement (Block of 4)
F1188/00	2nd Fast Interface Enhancement (Block of 4)
F1189/00	3rd Fast Interface Enhancement (Block of 2)
F1190/00	1st High Speed Interface Enhancement (Block of 2)
F1191/00	2nd High Speed Interface Enhancement (Block of 2)
F1192/00	3rd High Speed Interface Enhancement (Single)

2.2.2 2082 OPTIONS

Type Number	Description
F1148/00	Extended Precision Floating Point Unit
F1149/00	Paging
F1184/00	1st Slow Interface Enhancement (Block of 6)
F1185/00	2nd Slow Interface Enhancement (Block of 8)
F1397/00	2 Fast Interfaces - 1st Enhancement
F1437/00	2 Fast Interfaces - 2nd Enhancement
F1438/00	2 Fast Interfaces - 3rd Enhancement
F1439/00	2 Fast Interfaces - 4th Enhancement
F1440/00	2 Fast Interfaces - 5th Enhancement
F1441/00	2 High Speed Interfaces - 1st Enhancement
F1442/00	2 High Speed Interfaces - 2nd Enhancement
F1443/00	1 High Speed Interface - 3rd Enhancement

2.3 Conversions

Type Number	Description
C1056/00	Conversion of 2080/02 to 2080/03
C1057/00	Conversion of 2080/03 to 2080/04
C1058/00	Conversion of 2080/04 to 2080/05
C1059/00	Conversion of 2080/05 to 2080/06

2.4 Basic Accessories

The items listed below are provided, free of charge, with each Central Processor.

Description	Qty	
Console Chair	1	
Console Typewriter Stationery ($8\frac{1}{2}$" x 200" poll, 2 part)	2	1 per each Console Typewriter
Console Typewriter Ribbons	2	

Additional supplies may be obtained from Dataset at their current prices.

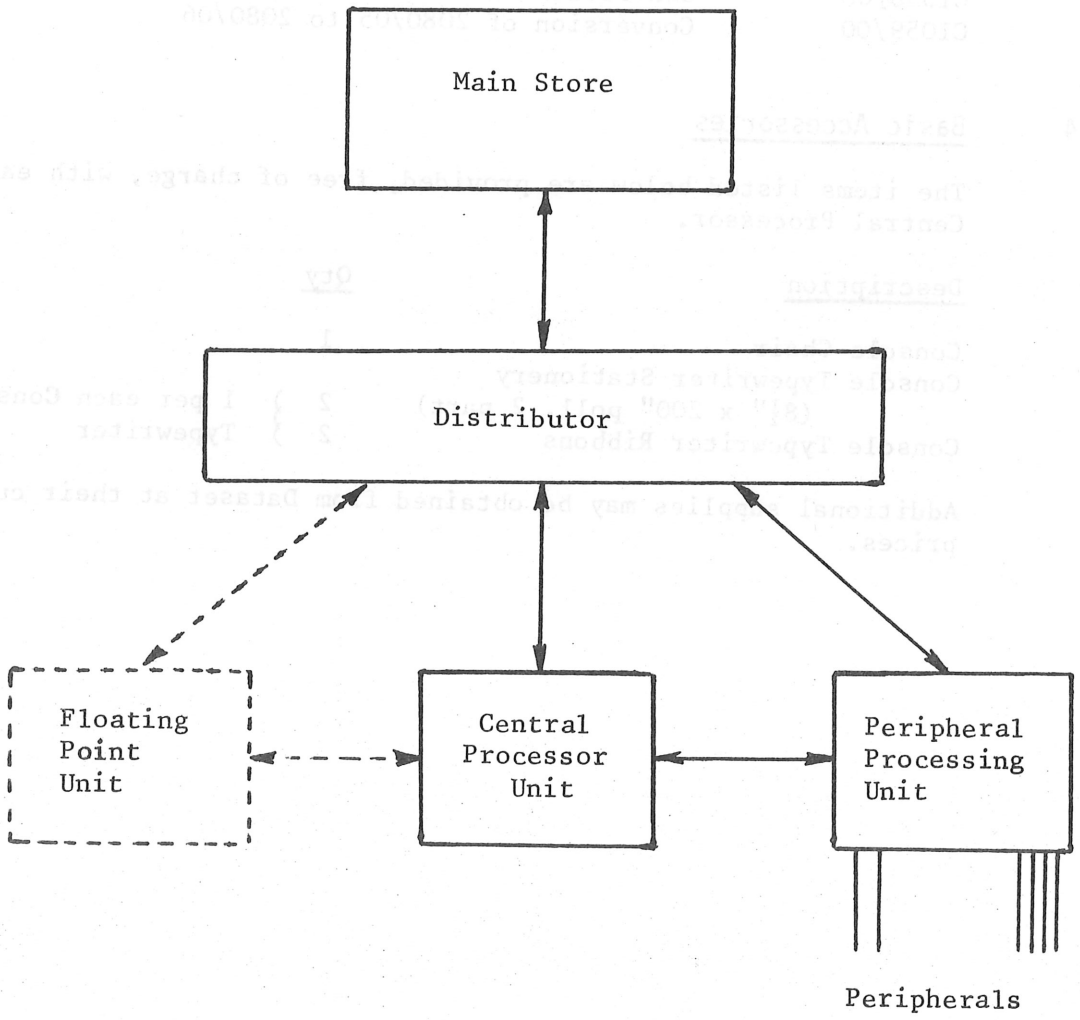


FIGURE 1 Logical structure of 1906A

3.0 CONNECTIVITY

3.1 Major Units

The Central Processor Unit, Peripheral Processing Unit and Floating Point Unit (if fitted) are connected to Main Store via a Distributor, see Figure 1.

The Main Store comprises modules of 32K words which are connected in pairs to 50 bit wide store interfaces of which there are either 2 or 4 depending on the total store size and degree of interleaving as illustrated in Figures 2 - 6.

3.2 Peripheral Connectivity

3.2.1 There are three aspects of connectivity relating to the attachment of 1900 Series peripherals to 1906A that must be satisfied:

a) All connected peripherals must be supported by the Executive (s) to be used with the system.

b) The correct type of Standard Interface must be provided for the connection of each peripheral.

c) The total peripheral configuration must be able to run with simultaneity.

To satisfy requirement a) it is necessary to determine the type of Executive (s) to be used by reference to 4.0 below, then to refer to the Approved Central Processor/Peripheral Connections table given in Appendix A to determine whether any given peripheral(s) is (are) supported by that Executive(s). To satisfy requirements b) and c) use the information given in 3.2.3 below in conjunction with the 1906A & 1906S Peripheral Simultaneity Rules given in Appendix B.

3.2.2 I/O CHANNELS & PERIPHERAL SIMULTANEITY

3.2.2.1 The 1906A and 1906S Peripheral Simultaneity Rules determine the types of Standard Interface channels that can be used with different types of peripherals on these processors and give the loading value (IMTAC Value) applicable to each peripheral. Tables 1 and 2 below show the interfaces available with the 2080 and 2082 versions of 1906A and the sequence in which they must be ordered.

STORE INTERLEAVING SHOWING LAYOUT OF ABSOLUTE ADDRESSES

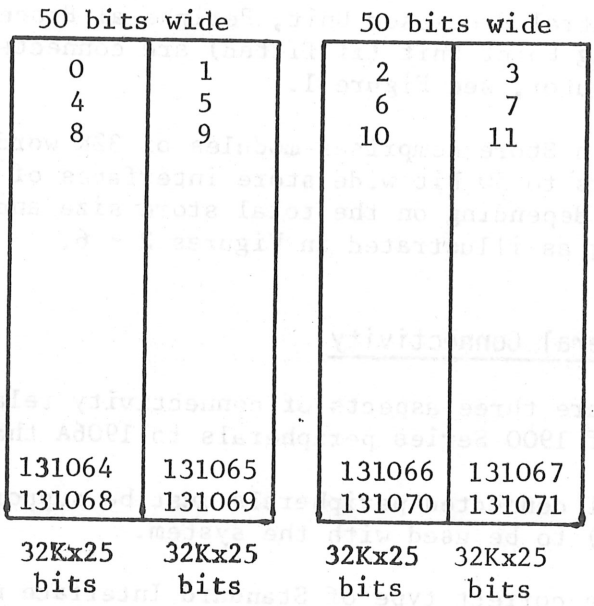
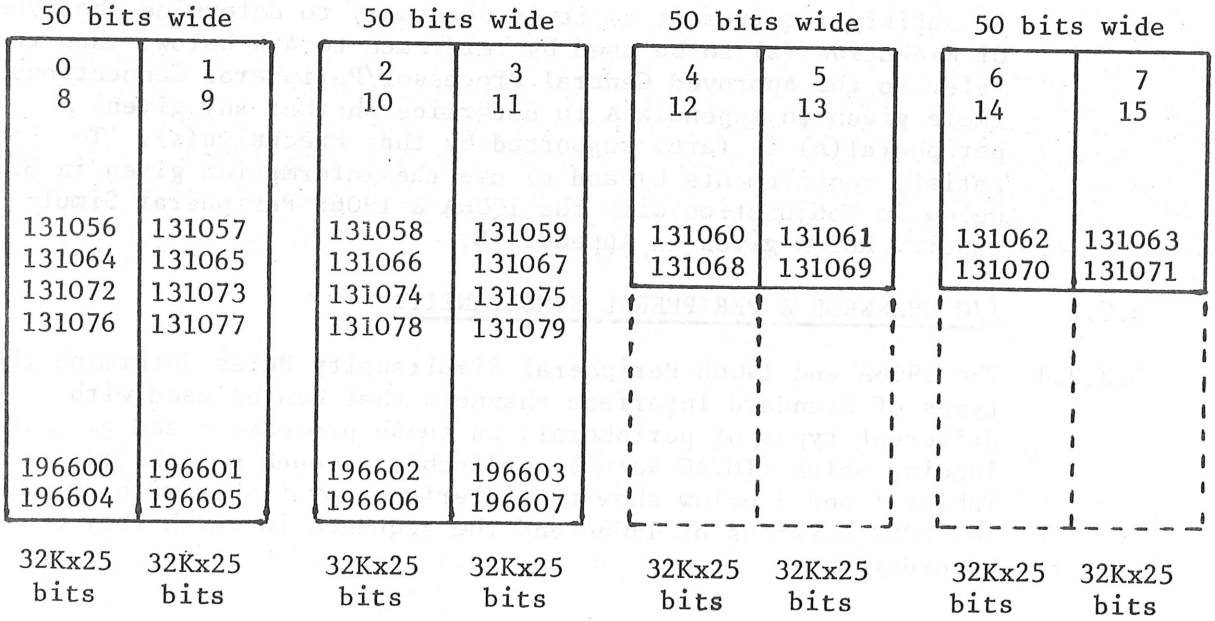


FIGURE 2 128K Store, 2-way interleaved



N.B. 256K supplied but only 192K used by customer.

FIGURE 3 192K Store, 4-way interleaved up to 128K, 2-way interleaved from 128K to 192K

TABLE 1 Interfaces available on the 2080 Central Processor

Sequence of ordering	Slow Interfaces No. in Block	Slow Interfaces Type Number	Fast Interfaces No. in Block	Fast Interfaces Type Number	High Speed Interfaces * No. in Block	High Speed Interfaces * Type Number
Basic 2080	10	-	4	-	-	-
1st Enhancement	6	F1184	4	F1187	2	F1190
2nd Enhancement	8	F1185	4	F1188	2	F1191
3rd Enhancement	6	F1186	2	F1189	1	F1192

TABLE 2 Interfaces available on the 2082 Central Processor

Sequence of ordering	Slow Interfaces No. in Block	Slow Interfaces Type Number	Fast Interfaces No. in Block	Fast Interfaces Type Number	High Speed Interfaces * No. in Block	High Speed Interfaces * Type Number
Basic 2082	10	-	4	-	-	-
1st Enhancement	6	F1184	2	F1397	2	F1441
2nd Enhancement	8	F1185	2	F1437	2	F1442
3rd Enhancement	-	-	2	F1438	1	F1443
4th Enhancement	-	-	2	F1439	-	-
5th Enhancement	-	-	2	F1440	-	-

* If all Fast Interface blocks have been used and more are required then any of the High Speed Interface Blocks may be used as additional Fast Interface Blocks. Such use must be clearly stated on all quotation forms and order forms.

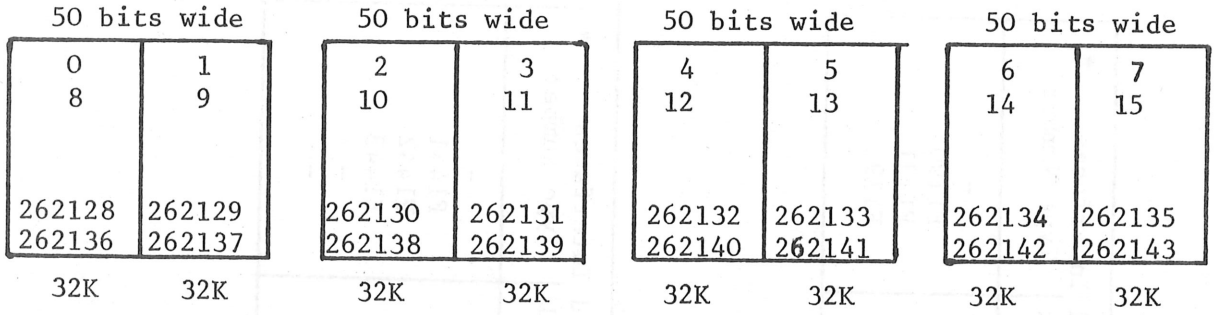


FIGURE 4 256K Store, 4-way interleaved

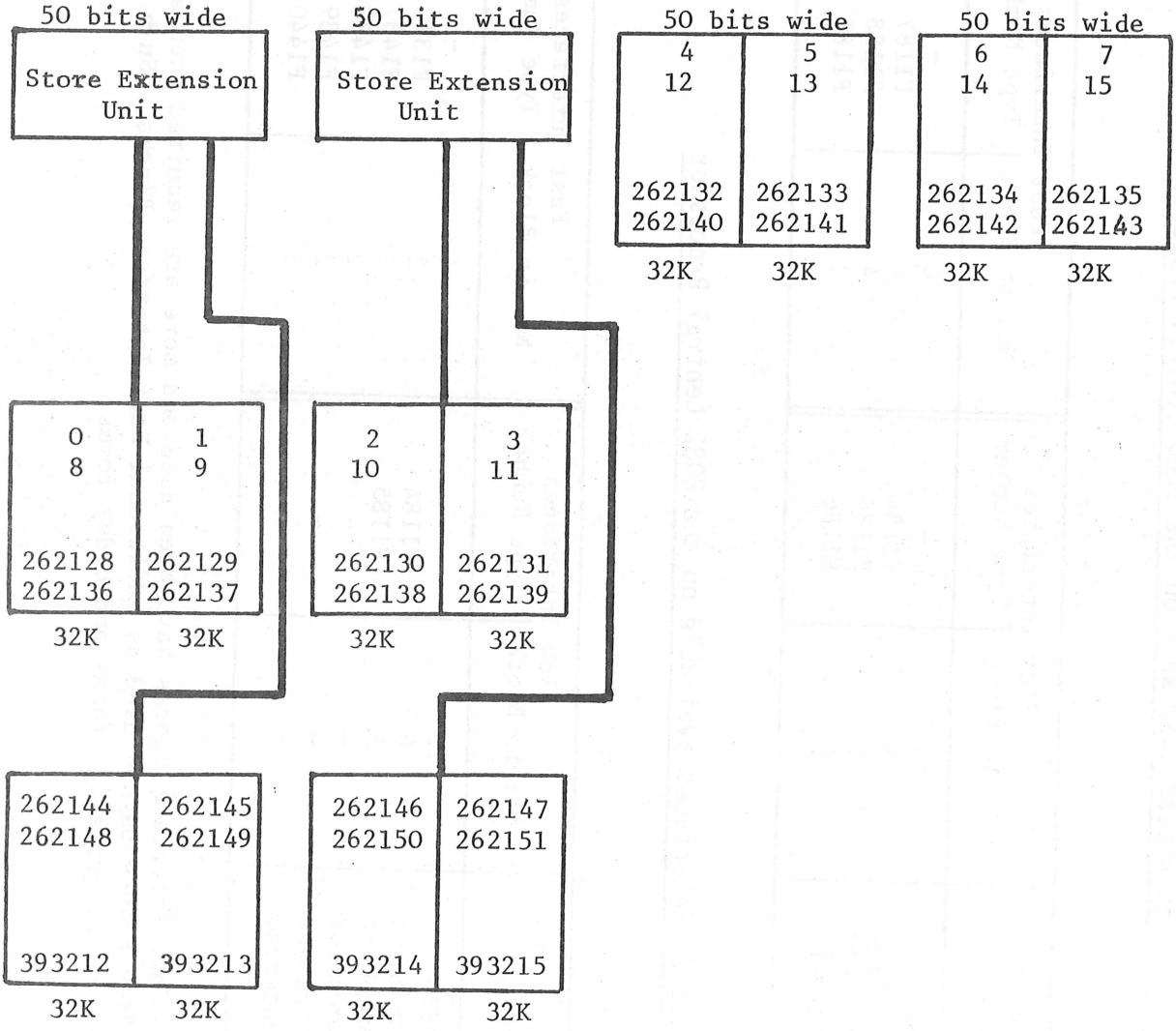


FIGURE 5 384K Store, 4-way interleaved up to 256K, 2-way interleaved from 256K to 384K

3.2.2.2 The maximum peripheral loading values permitted on 1906A are as follows:-

Maximum IMTAC value allowed per block of High Speed Interfaces;

a) 2080 system	375
b) 2082 system	750

Maximum IMTAC value allowed per block of Fast Interface, or per block of High Speed Interfaces used Fast Interfaces. 112.5
Maximum IMTAC value allowed for all Slow Interfaces 200

Maximum IMTAC value allowed per system;

a) 2080 system	1250
b) 2082 system	1625

4.0 EXECUTIVE

4.0.1 The following Executives may be used with a 1906A:

EWG3 (with GEORGE 3) - unpaged system or paging switched OFF

EWG4 (with GEORGE 4) - paged system with paging switched ON.

For further details of Executive, including compile-time options, store occupancy and peripheral requirements see Section 2.

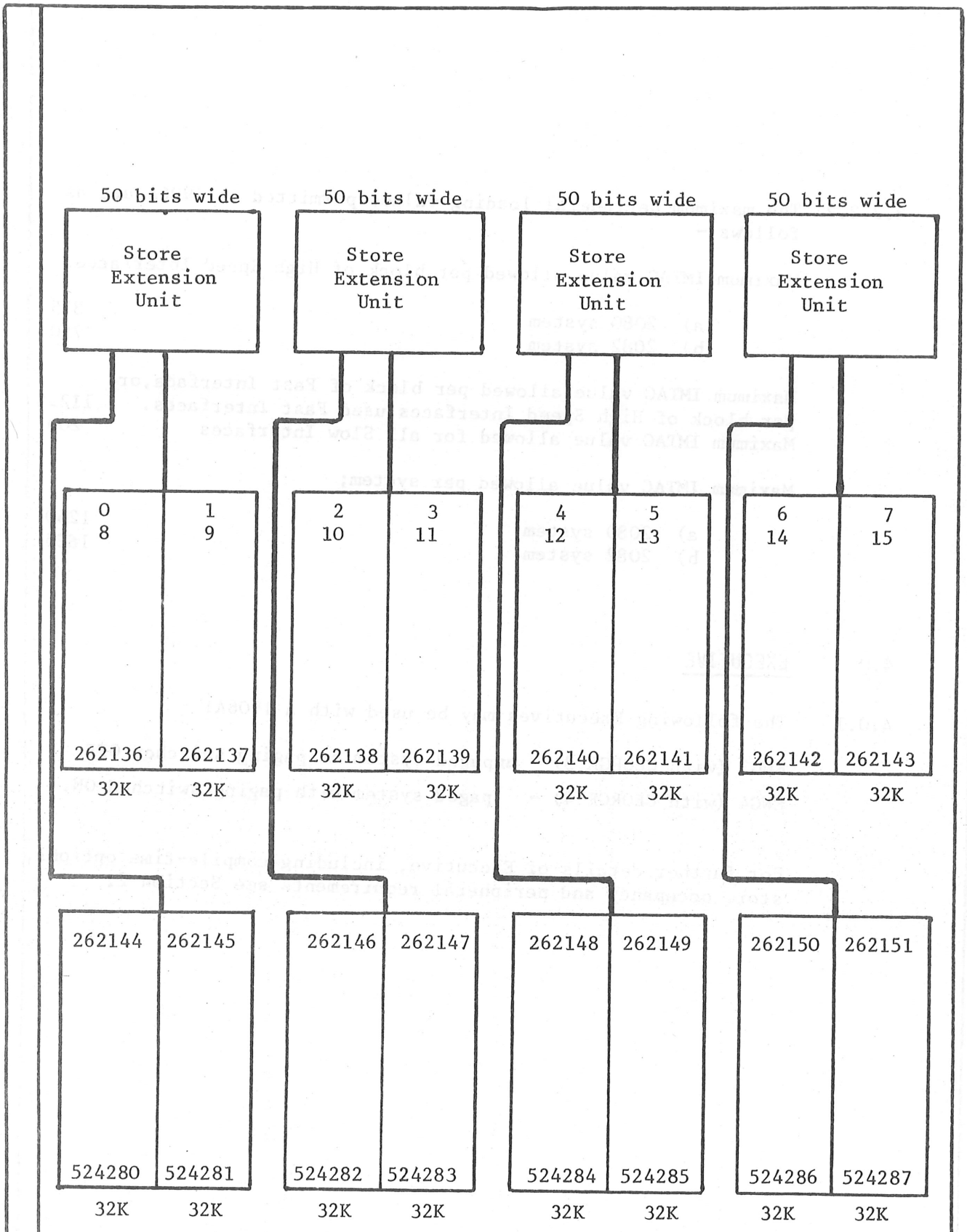


FIGURE 6 512K Store, 4-way interleaved

5.0 HARDWARE GENERAL DESCRIPTION

5.1 System Description

5.1.1 The 1906A comprises a Central Processor Unit (CPU), a Peripheral Processor Unit (PPU) and, if fitted, an optional hardware Floating Point Unit (FPU). All of these units have direct access to main store through a distributor; see Fig. 1. The CPU controls the overall operation of the system and initiates the independent autonomous activities of the PPU and FPU.

5.1.2 The CPU fetches instructions from main store, decodes and executes them. Floating-point instructions will either cause an interrupt to Executive and be performed by extracodes or, if an FPU is fitted, will be passed on to the FPU for execution. All peripheral transfers are handled by the PPU with intervention from the CPU only at the beginning and end of each block transfer.

5.1.3 Emitter-Coupled Logic (ECL) technology is used throughout the CPU, PPU and FPU. The circuit modules are mounted on multi-layer platters designed to provide impedance matched interconnections. The main store is core store.

5.2 Central Processor Unit

5.2.1 The CPU is of asynchronous design with overlapped instructions and includes hardware accumulators, a Real Time Clock and an Instruction Operand Counter as standard. It implements the 1900 Series order code to C2 level with up to 8 instructions held in the pipeline in course of execution at one time. For a list of instructions and timings see 8.0.

5.2.2 The addressing capability of the CPU is up to 4M words with the Paging Option, see 5.2.6, however the physical size of main store that can be attached is limited by the address distributor to 512K words.

5.2.3 REAL TIME CLOCK

Causes an interrupt to Executive every 10 milliseconds.

5.2.4 INSTRUCTION OPERAND COUNTER

Counts the number of operand phases of all instructions obeyed while the processor is in Object Program Mode. The counter adds one for each operand phase of an instruction except for floating point operands when it adds 2.

5.3.5 CPU PERFORMANCE DEGRADATION DUE TO PERIPHERAL TRANSFERS

The demand for store accesses will increase with peripheral activity and, due to clashes, will increase the average time that the CPU takes to process instructions. Performance degradation will vary depending upon the degree of store interleaving and on the type of data transfer i.e. whether it is single character or 4-character. Percentage CPU degradation is of the order:

a) For single-character transfers;

0.075% per 1K Chs/second for 2 way interleaved store.
0.045% per 1K Chs/second for 4 way interleaved store.

b) For 4-character transfers;

0.5% per 100K Chs/second for 2 way interleaved store.
0.3% per 100K Chs/second for 4 way interleaved store.

The above figures are based on the statistically likely results taking into account that both the CPU and PPU need store for only a fraction of the total time available.

5.4 Main Store

5.4.1 The Main Store comprises 32K word modules of $2\frac{1}{2}$D construction core store with a cycle time of 750 nanoseconds. The modules are paired to provide a 50 bit wide store interface and these pairs of modules are either 2-way or 4-way interleaved depending on the total store size. For details of interleaving see Figures 2 to 6. In the case of failures, modules may be isolated and the remaining store reconfigured if necessary with reduced interleaving or without interleaving and provided sufficient store remains, work can then proceed. Self test facilities are provided for an engineer to test any isolated modules.

5.4.2 The minimum store that must be isolated in the case of a failure will depend on the store configuration and how it is to be reconfigured but cannot be less than 64K words i.e. a pair of modules. It should be noted that in the case of a 192K word store, 256K words (8 x 32K word modules) are supplied of which the customer is allowed to use only 192K words, and, in the event of a failure, reconfiguration is permitted such that any 6 modules can be used non-interleaved. This still leaves the customer with 192K words of store available to him.

6.0 PHYSICAL CHARACTERISTICS

The 2080 and 2082 versions of 1906A differ in the way the cabinet assemblies are laid out. For details see Figures 7 and 8.

6.1 Dimensions & Weights

	Height	Depth	Length	Weight (approx)
Logic Bay	76"	44"	74"	2680 lbs
Power Supply Bay	76"	44"	74"	2820 lbs
Store Bay	76"	44"	74"	
Cooling Bay	76"	44"	54"	1460 lbs

6.2 Power Requirements

6.2.1 The system requires 2 Motor Alternators, one to provide a 400Hz supply for the CPU, the other to provide a regulated 50Hz supply for the core store and the remainder of the configuration. The processor and store impose the follwoing loadings:

CPU + PPU	54KVA	400 Hz
FPU	8KVA	400 Hz
128K	7.5KVA	50 Hz
192K	15KVA	50 Hz
256K	15KVA	50 Hz
384K	22.5KVA	50 Hz
512K	30KVA	50 Hz

6.2.2 The mains supply required is 3 phase 50 Hz with a nominal voltage in the range 220-250/382-433V.

6.3 Environment

Temperature range	$21^{o}C \pm 2^{o}C$ Ambient
Relative Humidity	50% $\pm$ 5% RH
Cleanliness	95% efficiency at particle size down to 1 micron.

The cooling units require a supply of chilled water; for a maximum CPU configuration the requirements are:

91 gals/min at $7^{o}C \pm 2^{o}C$.

6.4 Site Layout

CED Environmental Engineering should be consulted regarding all site layout details.

Cooling Bay	Power Supply Bay	Power Supply Bay	Power Supply Bay	Cooling Bay

Cooling Bay	Peripheral Processing Unit	Central Processor Bay	Central Processor Bay	Cooling Bay

Cooling Bay	Store Bay 128K max.	Store Bay 128K max.	Store Bay 128K max.	Store Bay 128K max.	Cooling Bay

FIGURE 7 2080 Plan view of bay assemblies

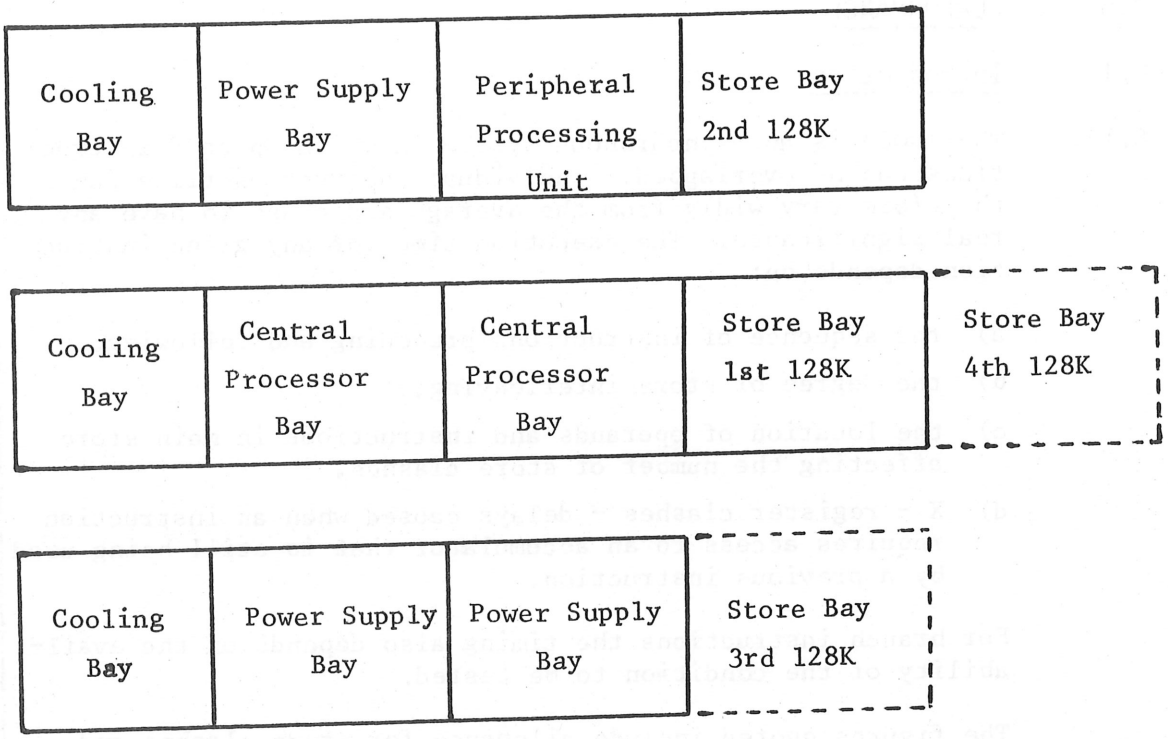


FIGURE 8 2082 Plan view of bay assemblies

7.0 FIELD ENHANCEMENTS

Because of the small number of 1906As of any one type field enhancement documentation is produced only when an enhancement is ordered. For details of the work involved in fitting any enhancement, estimated system down-time, testing time, etc. contact CED.

8.0 PERFORMANCE

8.1 Introduction

8.1.1 The 1906A is an asynchronous system in which up to 8 instructions can be overlapped. Individual instruction times can therefore vary widly from the average and cease to have any real significance. The execution time for any given instruction depends on:

a) the sequence of instructions preceding and following,

b) the degree of store interleaving,

c) the location of operands and instructions in main store affecting the number of store clashes,

d) X - register clashes - delays caused when an instruction requires access to an accumulator that is still being used by a previous instruction.

For branch instructions the timing also depends on the availability of the condition to be tested.

The figures quoted include allowance for store clashes and, for branch instructions, are dependent on the condition to be tested being immediately available. No allowance is made for X - register clashes. The effect of these is strongly dependent on the detailed coding of a particular program and could cause variations of up to 20%.

8.1.2 A more meaningful indication of the central processor speed is given by the time taken to perform various instruction loops or sequences; some such times are quoted for specified loops.

8.1.3 Performance may be degraded due to peripheral transfers; for details see page 610.14 para 5.3.5 . The processor performance will also be degraded if the main store exceeds 256K words; for the 384K word store degradation will be approximately 9% and for the 512K word store degradation will be approximately 18%.

8.2 Work Mix Times & Loop Times

The following timings are applicable to a system having a 4-way interleaved store not exceeding 256K words.

POWU II	0.93 milliseconds
Loop 1	4.07 microseconds
Loop 2	4.71 "
Loop 3	3.73 "

GAMM Mix (with H/W option F1148/00)

a)	Normal precision, Compact Mode	2.9	Microseconds
b)	Normal precision, Extended Mode	3.3	"
c)	Extended precision, Compact Mode	5.0	"
d)	Extended precision, Extended Mode	5.2	"

Loop 4	Scalar Product	5.79	Microseconds
Loop 5	Polynomial (Compact store, Single precision)	2.62	"
Loop 6	Polynomial (Extended store, Single precision)	2.99	"
Loop 7	Polynomial (Compact store, Double precision)	3.54	"
Loop 8	Polynomial (Extended store, Double precision)	3.90	"
Loop 9	Line by line compare of tables (Compact store)	5.11	"
Loop 10	Line by line compare of tables (Extended store)	5.05	"

Loops 1-10 are defined as follows:-

Loop 1	000	5	1/A
	011	5	2/B
	101	1	3/1
	001	2	3
	001	6	3/C
	060	3	S-5
Loop 2	001	7	5
	000	5	1/A
	041	5	2/B
	101	1	1
	101	2	1
	066	4	S-5
Loop 3	000	7	1/A
	101	1	1
	011	7	2/B
	101	2	1
	066	4	S-4
Loop 4	137	0	8N
	137	2	8N+2
	136	0	1/8A
	134	1	2/8B+2
	132	2	8N
	101	1	4
	101	2	4
	066	4	S-7
Loop 5	132	0	1/TABLE
	134	0	CONS
	062	1	S-2

First instruction assumed to be in location 8M where N and M are any number.

```
Loop 6    132   0    1/TABLE
          134   Ø    CONS
          101   1/2
          066   4    S-3

Loop 7    132   2    1/TABLE
          134   2    CONS
          062   1    S-2

Loop 8    132   2    1/TABLE
          134   2    CONS
          101   1/2
          066   4    S-3

Loop 9    136   0    2/TABLE
          133   0/4
          076   1/DIFF
          062   2      S-3

Loop 10   136   0    3/TABLE
          133   0/4
          076   1/DIFF
          101   3/2
          066   2    S-4
```

8.3 Basic Function Code & Timings

The timings quoted below are based on the average time to perform an instruction when it is repeated a large number of times. In some cases this is equal to the function execution time, i.e. time in arithmetic unit or other logic unit, since all instructions fetching and preparation time is lost in the overlap.

All branch instructions are dependent on the condition to be tested being immediately available.

Function Number	Function Name	2-way interleaved	4-way interleaved
000	LDX	1.1 usec	0.86 usec
001	ADX	1.1	0.86
002	NGX	1.1	0.86
003	SBX	1.1	0.86
004	LDXC	1.1	0.86
005	ADXC	1.1	0.86
006	NGXC	1.1	0.86
007	SBXC	1.1	0.86
010	STO	1.9	1.55
011	ADS	1.9	1.55
012	NGS	1.9	1.55
013	SBS	1.9	1.55
014	STOC	1.9	1.55
015	ADSC	1.9	1.55
016	NGSC	1.9	1.55
017	SBSC	1.9	1.55
020	ANDX	1.1	0.86
021	ORX	1.1	0.86
022	ERX	1.1	0.86
023	OBEY (1)	1.4/0.86	1.4/0.86
024	LDCH	1.1	0.86
025	LDEX	1.1	0.86
026	TXU	1.1	0.86
027	TXL	1.1	0.86
030	ANDS	1.9	1.55
031	ORS	1.9	1.55
032	ERS	1.9	1.55
033	STOZ	1.9	1.55
034	DCH	1.9	1.55
035	DEX	1.9	1.55
036	DSA	1.9	1.55
037	DLA	1.9	1.55
040	MPY	1.7	1.7
041	MPR	1.7	1.7
042	MPA	1.7	1.7
043	CBD	1.1	0.86
044	DVD (2)	3.5	3.5
045	DVR	3.5	3.5
046	DVS	3.5	3.5
047	CBD	1.9	1.55

(1) The two times quoted correspond to whether the 023 is in an even or odd store location.

(2) These instructions will be extended by 0.5usec if the operands are such that end corrections are necessary.

Function Number	Function Name	4 and 2 way interleaved		
		No Jump	Jump in even	Jump in Odd
050	BZE	0.94	1.4	1.0
052	BNZ	0.94	1.4	1.0
054	BPZ	0.94	1.4	1.0
056	BNG	0.94	1.4	1.0
060	BUX	0.94	1.4	1.0
062	BDX	0.94	1.4	1.0
064	BCHX	0.94	1.4	1.0
066	BCT	0.94	1.4	1.0
070	CALL	-	1.7	1.1
072	EXIT	-	1.4	1.0
074	BRN etc.	0.94	1.4	1.0
100	LDN		0.55	
101	ADN		0.55	
102	NGN		0.55	
103	SBN		0.55	
104	LDNC		0.55	
105	ADNC		0.55	
106	NGNC		0.55	
107	SBNC		0.55	
110	SLC (3)		0.55	
111	SLC (3)		0.55	
112	SRC (3)		0.55	
113	SRC (3)		0.55	
114	NORM (3)		0.55	
115	NORM (3)		0.55	

(3) Shifts are done in units of 1 and 3 places, each taking 50 nsecs. For shifts in excess of 6 places, add 50 nsecs per unit to the specification time of 0.55 microsecs.

Function Number	Function Name	2-way interleaved	4-way interleaved
116	MVCH (4)	1.9+2.5n	1.9+2.5n
117	SMO	1.5	1.2
120	ANON	0.55	0.55
121	ORN	0.55	0.55
122	ERN	0.55	0.55
123	NULL	0.55	0.55
124	IDCT	0.55	0.55
125	MODE (5)	6.0	6.0
126	MOVE (6)	$1.9+1.45\frac{n}{2}$	$1.9+1.3\frac{n}{2}$
127	SUM	1.2+1.1n	1.2+1.1n

(4) n refers to number of characters to be moved. For read/write areas in the same store module, both times will be extended to (1.6 + 2.5n) u sec.

(5) The time for MODE can vary considerably as all current instructions in the CPU must be completed . The time quoted, 5 u sec, is an estimated average time.

(6) n refers to numbers of words, or pairs of words, to be moved.
Move is done in pairs, hence $\frac{n}{2}$, if starting and ending addresses are both odd or both even.

Further, these times assume the move is between different store blocks; if the same block, the basic time becomes $(1.6 + 1.6\frac{n}{2})$ u sec.

If these conditions are not met (i.e. starting at an odd address and finishing at an even address or vice versa then $\frac{n}{2}$ becomes n).

8.4 Floating Point Unit Function Code & Timings

Normal Precision Operation

		2-way interleaved	4-way interleaved
130	FLOAT	1.1 microseconds	0.86 microseconds
131	FIX	1.3 "	1.2 "
132	FAD	1.2 "	1.1 "
133	FSB	1.3 "	1.1 "
134	FMPY	2.6 "	2.6 "
135	FDVD	6.5 "	6.5 "
136	LFP	1.1 "	0.86 "
137	SFP	1.3 "	1.2 "

Extended Precision Operation

132	1.7 microseconds	1.6 microseconds
133	1.7 "	1.6 "
134	4.1 "	4.1 "
135	11.8 "	11.8 "
136	1.7 "	1.6 "

The above times are those experienced if the same instruction is repeated a large number of times.

9.0 ORDER VETTING CHECKLIST

1. Check that the correct system number has been quoted.

2. Check that peripherals specified are supported by GEORGE 3/4 Executive. See Appendix A.

3. Check peripheral simultaneity and that the correct quantity and types of I/O channels have been specified for the connection of all peripherals. See 3.2 and Appendix B.

4. Where peripheral switches or communications equipment have been specified check that configuration diagrams have been supplied.

5. When peripherals are withdrawn ensure that the configuration still contains those required for maintenance purposes and by the Operating System. See 9.1 below and Section 2.0.

9.1 Mandatory Peripherals Required For Maintenance Purposes

INPUT DEVICE

Either an 80 column card reader or paper tape reader.

OUTPUT DEVICE

Line printer with 96 or more print positions.