1906S Processor

1.0 INTRODUCTION

1.0.1 The 1906S is the most powerful processor available in the 1900 Series. It is a large-scale, general-purpose machine designed to process both commercial and scientific applications. Systems may be configured from the components listed in 2.1 and 2.2 below and the peripherals listed in Appendix A. All connected peripherals must be able to run simultaneously and appropriate Standard Interfaces must be provided for them.

1.1 Summary of Characteristics

Order Code Level	C
Main Store Cycle Time	300 Nanoseconds
Main Store Size	128K - 512K words (plated wire store)
POWU II (4-way interleaved store)	0.65 milliseconds
GAMM Mix (with H/W option F1148/00)	
a) Normal precision	2.4 microseconds
b) Extended precision	3.6 microseconds
Total I/O throughput	11.0 M ch./seconds

2.0 TYPE NUMBERS & CONSTITUENT ITEMS

2.1 Standard Components

Type Number 2085/0 — Description: 1906S Central Processor comprising the following:-

a) Central Processor Unit (CPU) including:-

i) Hardware Accumulators
ii) Real Time Clock
iii) Instruction Operand Counter

b) Peripheral Processing Unit (PPU) including:-

i) 4 Fast Peripheral Standard Interfaces
ii) 10 Slow Peripheral Standard Interfaces

c) DC Power Supply Units and Cooling Units

d) Console Typewriter Desk with Console Typewriter

e) Spare Console Typewriter

2085/02	128K words of 300 Nsec. Store	size optional
2085/03	192K words of 300 Nsec. Store	
2085/04	256K words of 300 Nsec. Store	
2085/05	384K words of 300 Nsec. Store	
2085/06	512K words of 300 Nsec. Store	

2.2 Optional Hardware Features

Type Number	Description
F1148/00	Extended Precision Floating Point Unit
F1149/00	Paging
F1184/00	1st Slow Interface Enhancement (Block of 6)
F1185/00	2nd Slow interface Enhancement (Block of 8)
F1397/00	2 Fast Interfaces - 1st Enhancement
F1437/00	2 Fast Interfaces - 2nd Enhancement
F1438/00	2 Fast Interfaces - 3rd Enhancement
F1439/00	2 Fast Interfaces - 4th Enhancement
F1440/00	2 Fast Interfaces - 5th Enhancement
F1441/00	2 High Speed Interfaces - 1st Enhancement
F1442/00	2 High Speed Interfaces - 2nd Enhancement
F1443/00	1 High Speed Interface - 3rd Enhancement

2.3 Conversions

Type Number	Description
C1172	Conversion of 2085/02 to 2085/03
C1173	Conversion of 2085/03 to 2085/04
C1174	Conversion of 2085/04 to 2085/05
C1175	Conversion of 2085/05 to 2085/06

2.4 Basic Accessories

The items listed below are provided with the Central Processor.

Description	Qty.
Console Chair	1
Console Typewriter Stationery	2
Typewriter Ribbons	2

3.0 CONNECTIVITY

3.1 Major Units

The Central Processor Unit, Peripheral Processing Unit and Floating Point Unit (if fitted) are connected to Main Store via a Distributor, see Figure 1.

The Main Store comprises modules of 32K words which are connected to 50 bit wide store interfaces as illustrated in Figures 2 - 6. Note the modules may be configured either in pairs or as 2 x 16K words of 25 bits in order to connect to each 50 bit wide store interface.

3.2 Peripheral Connectivity

3.2.1 There are three aspects of connectivity relating to the attachment of 1900 Series peripherals to 1906S that must be satisfied:

a) All connected peripherals must be supported by the Executive (s) to be used with the system.

b) The correct type of Standard Interface must be provided for the connection of each peripheral.

c) The total peripheral configuration must be able to run with simulataneity.

To satisfy requirement a) it is necessary to determine the type of Executive(s) to be used by reference to 4.0 below, then to refer to the Approved Central Processor/Peripheral Connections table given in Appendix A to determine whether any given peripheral(s) is (are) supported by that Executive(s). To satisfy requirements b) and c) use the information given below in conjunction with the 1906A & 1906S Peripheral Simulataneity Rules given in Appendix B.

3.2.2 I/O Channels & Peripheral Simultaneity

3.2,2.1 The 1906A Peripheral Simultaneity Rules determine the types of Standard Interface channels that can be used with different types of peripherals on these processors and give the loading value (IMTAC Value) applicable to each peripheral. Table 1 over shows the interfaces available with the 1906S and the sequence in which they must be ordered.

3.2.2.2 The maximum peripheral loading values permitted on the 1906S are as follows:-

Maximum IMTAC Value permitted per block of High Speed Interfaces	750
Maximum IMTAC Value permitted per block of Fast Interfaces*	112.5
Maximum IMTAC Value permitted per all Slow Interfaces	200
Maximum IMTAC Value permitted per 1906S System	2750

* or for block of High Speed Interfaces used as Fast Interfaces.

4.0 EXECUTIVE

4.0.1 The following Executives may be used with 1906S:

EWG3 (with GEORGE 3) - unpaged system or paging switched OFF

EWG4 (with GEORGE 4) - paged system with paging switched ON.

For further details of Executive, including compile-time options. store occupancy and peripheral requirements see Section 2.

TABLE 1 Interfaces available on the 1906S Central Processor.

Sequence of ordering	Slow Interfaces		Fast Interfaces		High Speed Interfaces*	
	No. in block	Type Number	No. in block	Type Number	No. in block	Type Number
Basic 1906S	10	-	4	-	-	-
1st enhancement	6	F1184/00	2	F1397/00	2	F1441/00
2nd enhancement	8	F1185/00	2	F1437/00	2	F1442/00
3rd enhancement	-	-	2	F1438/00	1	F1443/00
4th enhancement	-	-	2	F1439/00	-	-
5th enhancement	-	-	2	F1440/00	-	-

* If all Fast Interface blocks have been used and more are required then any of the High Speed Interface Blocks may be used as additional Fast Interface Blocks. Such use must be clearly stated on all quotation forms and order forms.

5.0 HARDWARE GENERAL DESCRIPTION

5.1 SYSTEM DESCRIPTION

5.1.1 The 1906S comprises a Central Processor Unit (CPU), a Peripheral Processor Unit (PPU) and, if fitted, an optional hardware Floating Point Unit (FPU). All of these units have direct access to main store through a distributor; see Fig. 1. The CPU controls the overall operation of the system and initiates the independent autonomous activities of the PPU and FPU.

5.1.2 The CPU fetches instructions from main store, decodes and executes them. Floating-point instructions will either cause an interrupt of Executive and be performed by extracodes or, if an FPU is fitted, will be passed on to the FPU for execution. All peripheral transfers are handled by the PPU with intervention from the CPU only at the beginning and end of each block transfer.

5.1.3 Emitter-Coupled Logic (ECL) technology is used throughout the CPU PPU and FPU. The circuit modules are mounted on multi-layer platters designed to provide impendance matched interconnections. The main store is Plated wire.

5.2 CENTRAL PROCESSOR UNIT

5.2.1 The CPU is of asynchronous design with overlapped instructions and includes hardware accumulators, a Real Time Clock and an Instruction Operand Counter as standard. It implements the 1900 Series order code to C2 level with up to 8 instructions held in the pipeline in course of execution at one time. For a list of instructions and timings see 8.0.

5.2.2 The addressing capability of the CPU is up to 4M words with the Paging Option, see 5.2.6, however the physical size of main store that can be attached is limited by the address distributor to 512K words.

5.2.3 Real Time Clock

Causes an interrupt to Executive every 20 milliseconds.

5.2.4 Instruction Operand Counter

Counts the number of operand phases of all instructions obeyed while the processor is in Object Program Mode. The counter adds one for each operand phase of an instruction except for floating point operands when it adds 2.

A multi-operand order has an operand phase for each word (or character) transferred. The N part of a literal is regarded as an operand phase.

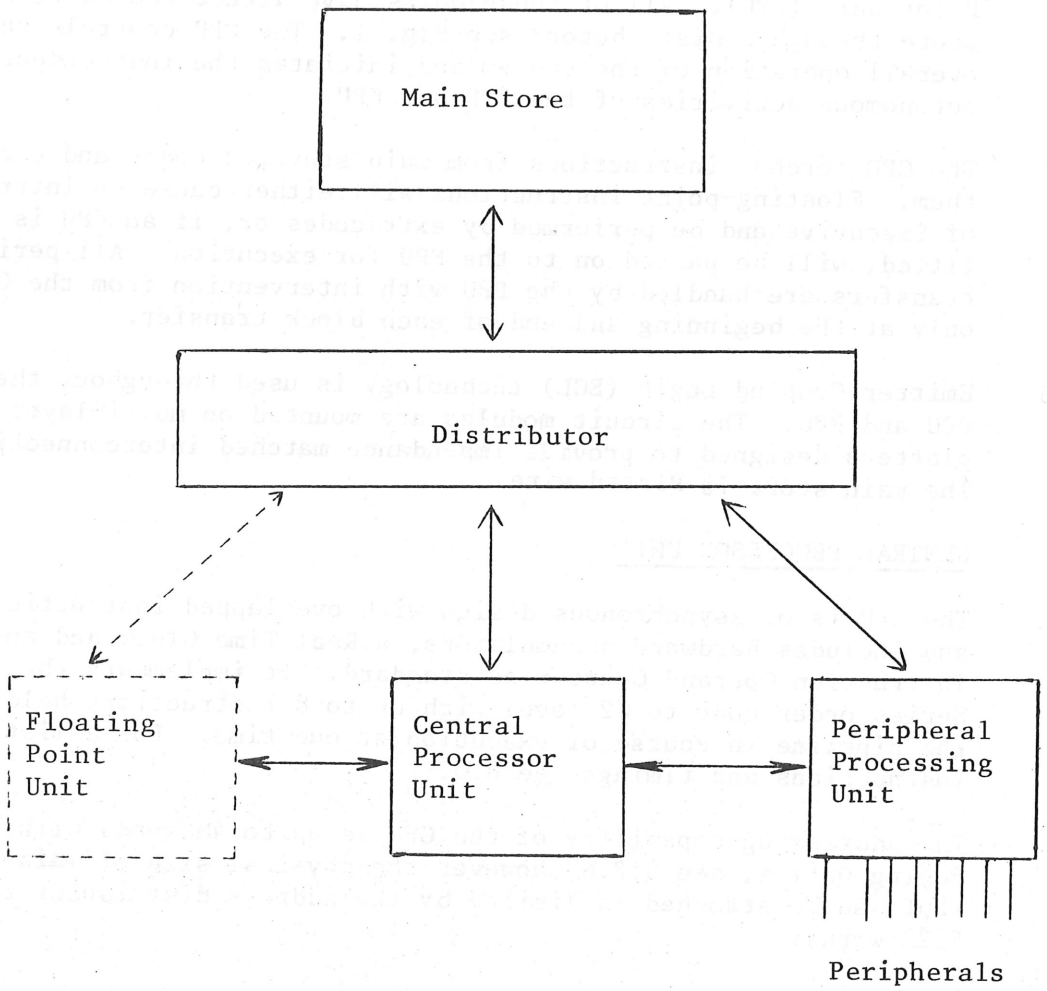

Figure 1 Logical structure of 1906S

5.2.5 Extended Precision Floating Point Unit (F1148/00)

The FPU can operate on both extended precision and normal precision floating point numbers with greater accuracy when rounding than was achieved with previous 1900 Series systems other than 1906A. Operating precision is determined by the values of X. The FPU operates auonomously with the CPU during the execution phase of floating point instruction.

5.2.6 Paging (F1149/00)

The Paging Feature enables a paged one-level store system to be implemented within addressing capability of up to 4M words. The one-level store is divided into blocks (pages) of 1K words which may reside in either main store or in backing store. A switch is provided to enable the processor to revert to datum/limit mode of operation. The additional hardware provided includes 16 Current Page Registers (CPRs).

To enable peripheral transfers to take place across page bounderies the PPU is fitted with Pointer Address Buffers which enable Control Word Buffers to be reloaded with a minimum of store accesses when a page boundary is reached.

5.3 PERIPHERAL PROCESSOR UNIT (PPU)

5.3.1 The PPU organises all store transfers associated with peripheral data and control words. It contains sufficient arithmetic logic to enable it to update counts, etc. without recourse to the arithmetic unit of the CPU and thus it is able to operate autonomously. Communication with the CPU is limited mainly to interrupts. The basic PPU includes a Slow Control and a Fast Control as standard. Additional Fast Controls and/or High Speed Controls may be added; these are provided with each block of Fast or High Speed Interfaces specified.

5.3.2 Slow Control

The Slow Control handles all single-character data transfers. It includes 10 Slow Peripheral Standard Interfaces as standard and may have additional blocks of Slow Peripheral Standard Interfaces added as indicated in Table 1 on page 620.4.

There is no buffering provided for Control Words and since these reside in main store, they must be accessed and updated by the PPU for every data character transferred. This requires 2 store cycles, the 1st is used to read the double-length Control Word and the last cycle is used to return the updated Control Word back to main store.

The data word containing the relevant character is read on the 2nd store cycle and, if the transfer is outwards to a peripheral no further data store cycles are required. However, if the data transfer is into store from a peripheral, the relevant character is input to the data word and the data word is written back to store on the 3rd store cycle. Thus 3 store cycles are used per

STORE INTERLEAVING SHOWING LAYOUT OF ABSOLUTE ADDRESSES

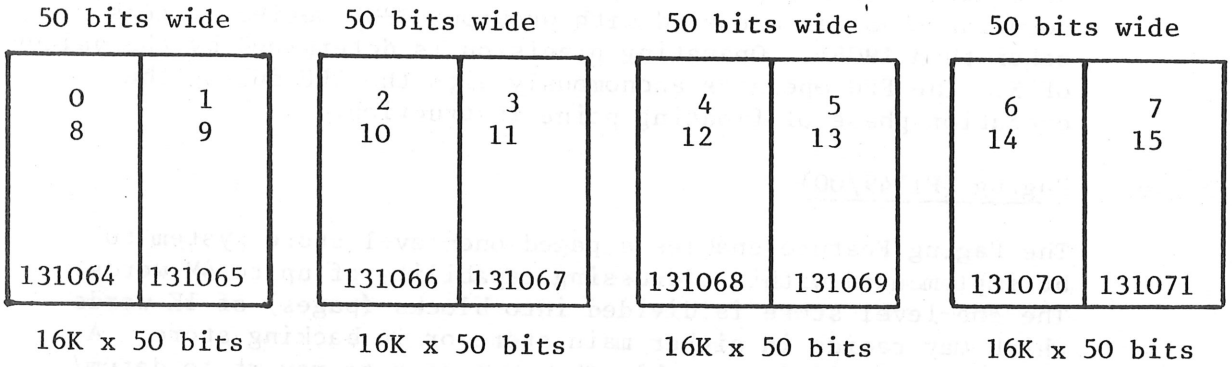

Figure 2 128K Store, 4-way interleaved

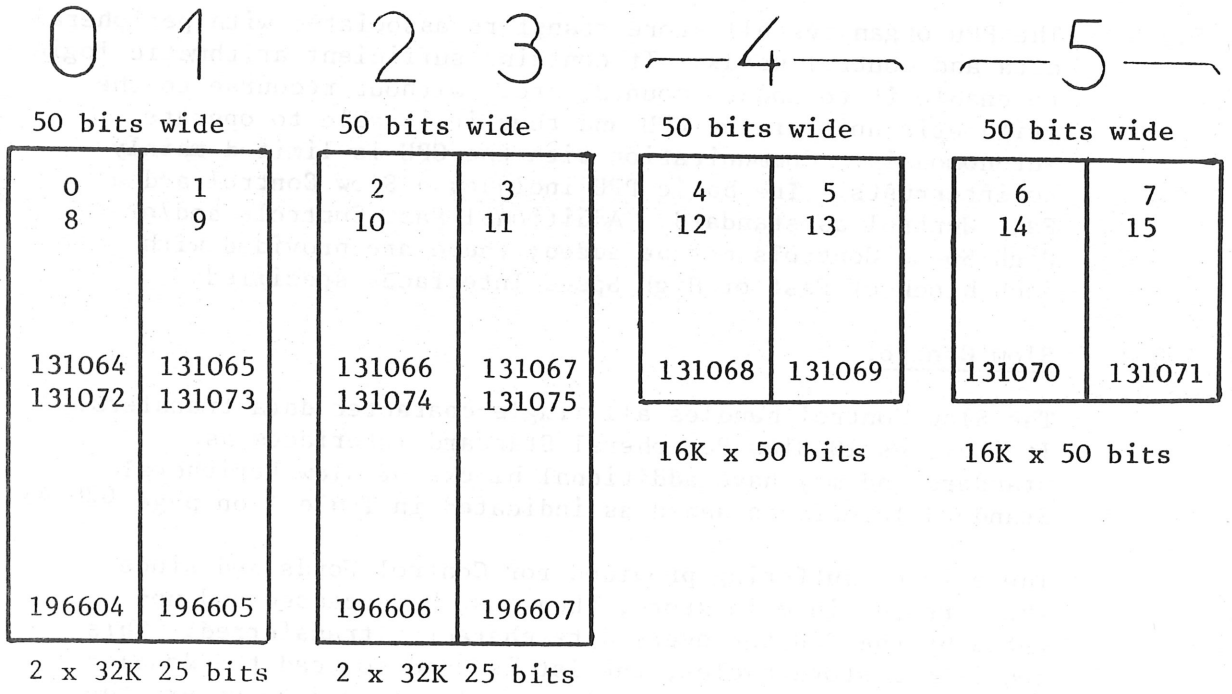

Figure 3 192K Store, 4-way interleaved up to 128K, 2-way interleaved from 128K to 192K

character written to a peripheral and 4 store cycles are used per character read from a peripheral. Single-character data transfers therefore load store comparatively heavily and the maximum permitted data rate of the Slow Control is limited to 50 K ch/second.

5.3.3 Fast Controls

Each block of Fast Peripheral Standard Interfaces is serviced by a Fast Control which is supplied automatically when the fast interface block is specified. The first Fast Control with 4 Fast Peripheral Standard Interfaces is provided as standard. Each Fast Control provides a double-word Data Buffer which is capable of transferring data at up to 450 Kchs/second. This data transfer rate may be achieved on any fast interface or block of fast interfaces connected to that Fast Control. The Fast Peripheral Standard Interfaces transfer data in burst mode and operate under F=0 timing rules. They may, therefore only be used for the connection of 4-character peripherals.

A double length Control Word Buffer is provided for each Fast Peripheral Standard Interface and block transfers are achieved using only one store cycle per data word transferred plus one cycle to read the Control Words at the beginning of the block and another cycle to return them to store at the end of the block.

5.3.4 High Speed Controls

Each block of High Speed Peripheral Standard Interfaces is serviced by a High Speed Control. None are provided as standard. Each High Speed Control provides a double-word Data Buffer and Control Word Buffers are provided for each High Speed Peripheral; Interface connected. Data transfers are handled in a similar manner to fast peripheral data transfers except that the High Speed Peripheral Standard Interfaces operate under F=1 timing rules at speeds of up to 1.5 M Chs/second subject to the overall limit imposed by the High Speed Control. The maximum data transfer rate per High Speed Control is 3.0 M Chs/second.

Any High Speed Control may be modified to allow the interfaces connected to it to operate under F=0 timing rules if required. In this case the maximum data transfer rate of the High Speed Control is reduced to 450K Chs/second. This modification is only permitted when all Fast Peripheral Standard Interface Enhancement Blocks have been specified and more Fast Peripheral Standard Interfaces are required.

5.3.5 CPU Performance Degradation Due to Peripheral Transfers

The demand for store accesses will increase with peripheral activity and, due to clashes, will increase the average time that the CPU takes to process instructions. Performance degradation will vary depending upon the degree of store interleaving and on the type of data transfer i.e. whether it is single character or 4-character. Percentage CPU degradation for a 4-way interleaved store is of the order:

a) For single-character transfers 0.04% per 1K Chs/second.

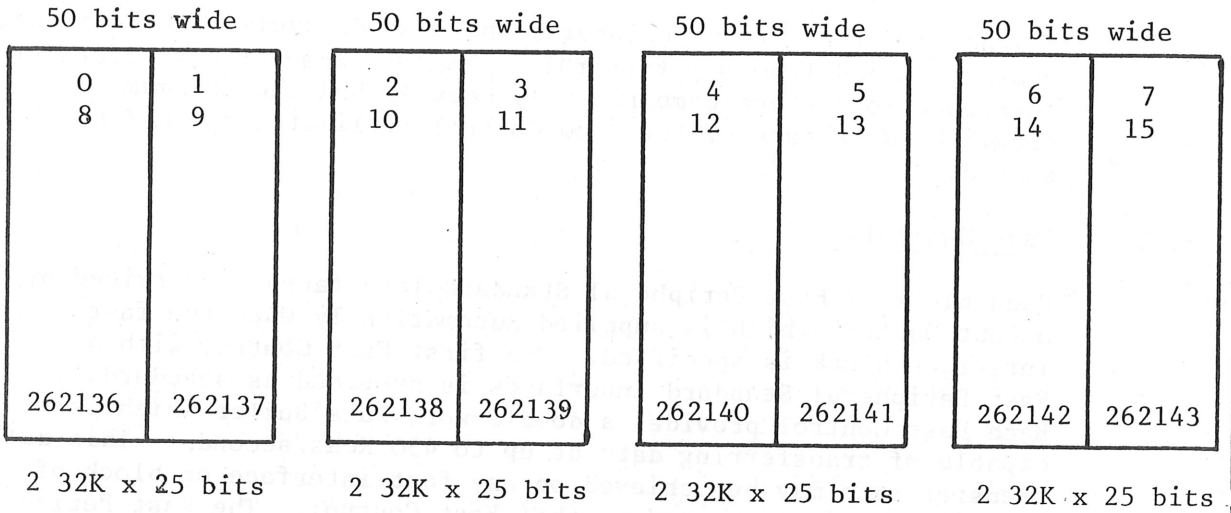

Figure 4 256K Store, 4-way interleave

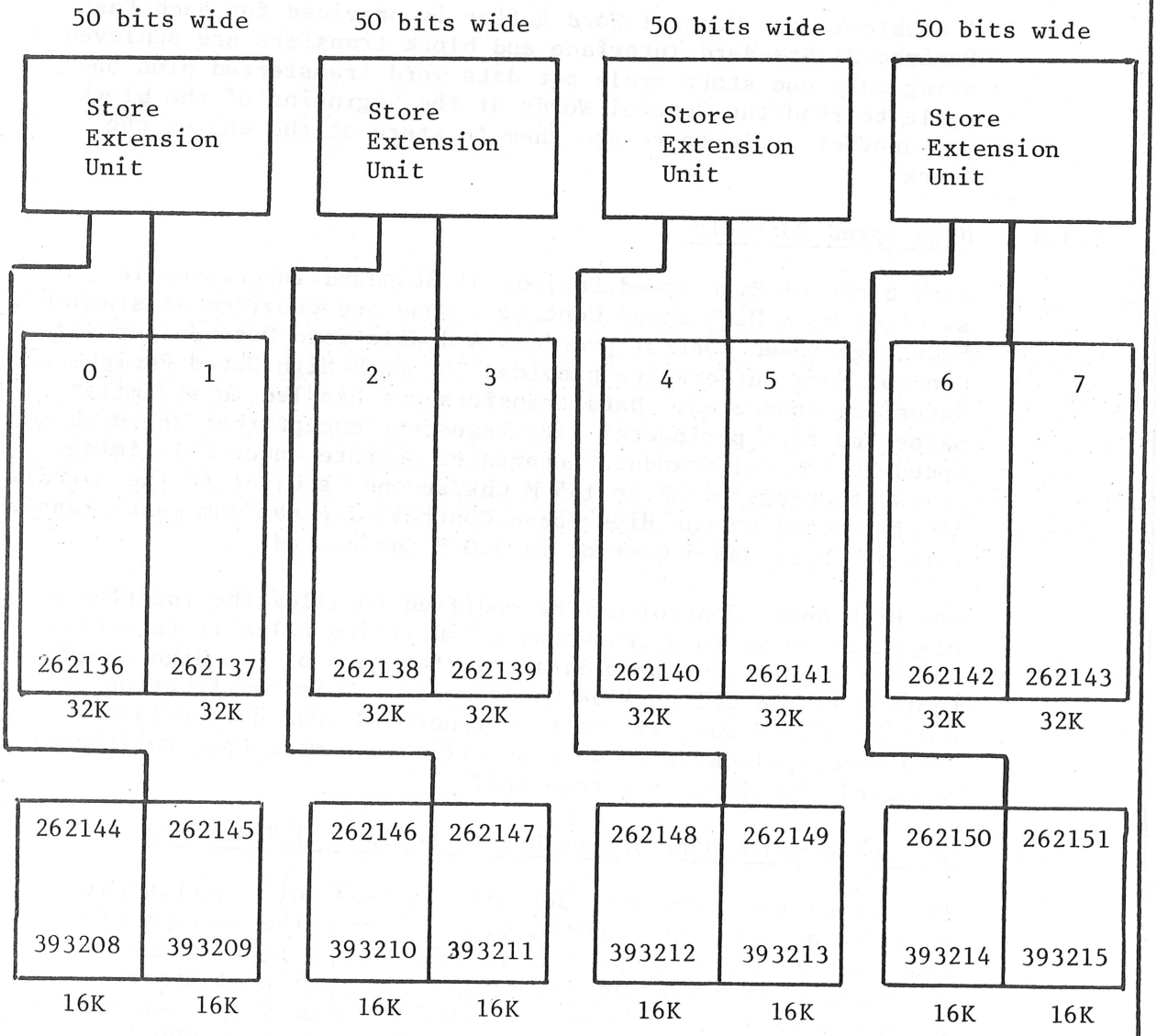

Figure 5 384K Store, 4-way interleaved

b) For 4-character transfers

(I)	via Fast Controls	0.25% per 100K Chs/second
(II)	via High Speed Controls	0.125% per 100k Chs/second*

* Applies whether the High Speed Control is used for High Speed or Fast Peripherals.

5.4 Main Store

5.4.1 The main store comprises 32K word modules of plated wire construction with a cycle time of 300 nanoseconds. The modules incorporate switches which may be set such as to provide either:

a) 32K words of 25 bits (24 data + 1 parity) or
b) 16K words of 50 bits (48 data + 2 parity)

depending on the way the store is interleaved; for details see Figures 2-6. In the case of failures, modules may be isolated and the remaining store reconfigured, if necessary with reduced interleaving or non-interleaved, and provided sufficient store remains, work can then proceed. Self test facilities are provided for an engineer to test isolated modules.

It should be noted that in the case of 192K word stores, unlike 1906A, only 192K words are supplied (see Figure 3) and in the case of a failure resilience is not as good as on 1906A. In Figure 3, modules 0, 1, 2 and 3 are configured as 32K word modules of 25K bits and modules 4 and 5 are configured as 16K word modules of 50 bits. The action of the reconfiguration switches is as follows:

Switch A interchanges modules 0, 1 with modules 2, 3
Switch B interchanges module 4 with module 5
Switch C interchanges modules 0, 1, 2, 3 with modules 4, 5

Consequently the resilience is as follows:

Module Failed	Reconfig'n Sw. Setting	Total store remaining	Interleaving
0	A $\overline{B}$ $\overline{C}$	64K	None
1	A $\overline{B}$ $\overline{C}$	64K	None
2	$\overline{A}$ $\overline{B}$ $\overline{C}$	64K	None
3	$\overline{A}$ $\overline{B}$ $\overline{C}$	64K	None
4	$\overline{A}$ $\overline{B}$ $\overline{C}$	128K	2-Way
5	$\overline{A}$ $\overline{B}$ $\overline{C}$	128K	2-Way

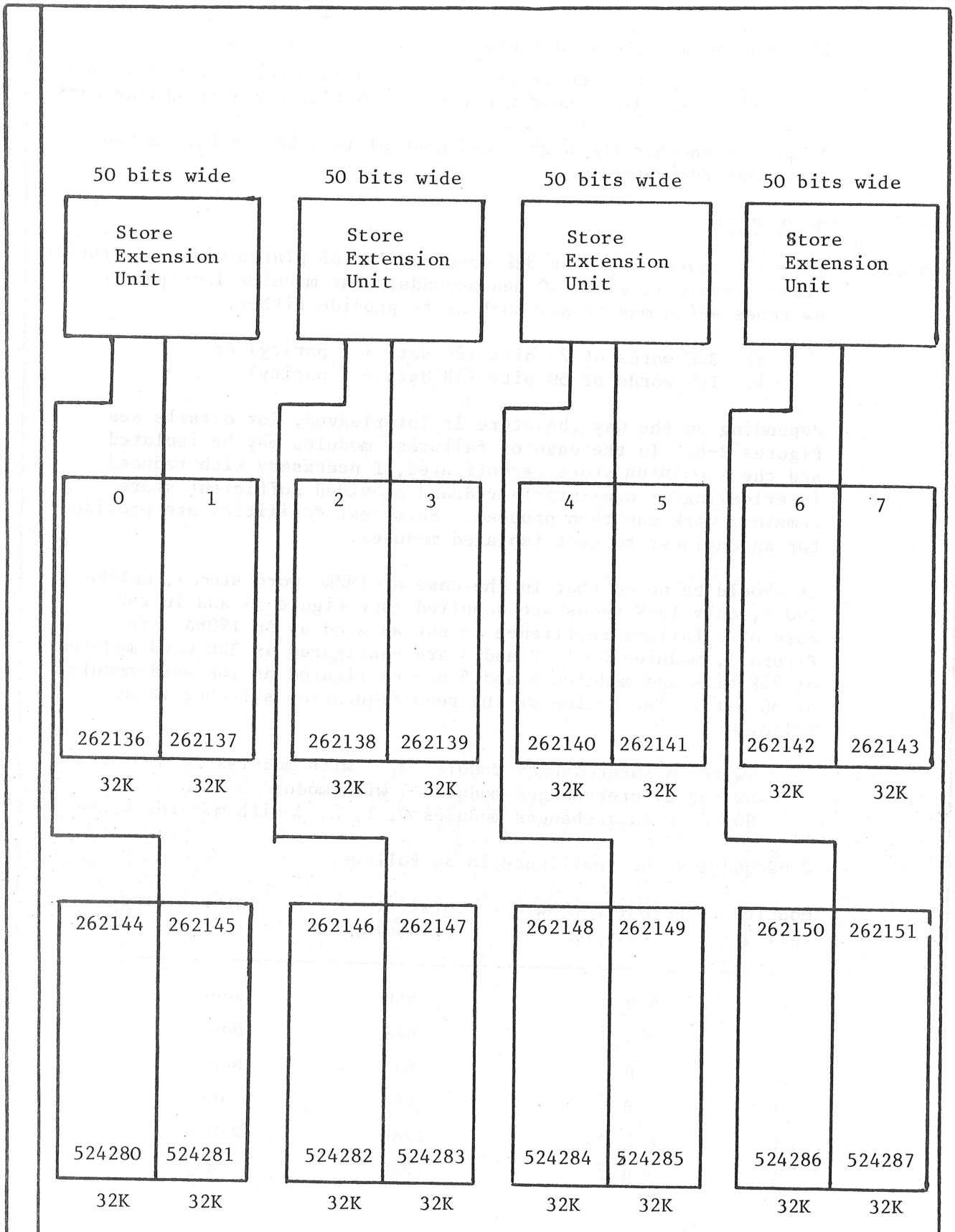

Figure 6 512K Store, 4-way interleaved

6.0 PHYSICAL CHARACTERISTICS

6.1 Dimensions & Weights

	Height	Depth	Length	Weight (approx)
Logic Bay	76"	44"	74"	2680 lbs
Power Supply Bay	76"	44"	74"	2820 lbs
Store Bay*	76"	44"	74"	3000 lbs
Cooling Bay	76"	44"	54"	1460 lbs

* Each Store bay can accomodate 8 store modules (256K words)

6.2 Power Requirements

6.2.1 The system requires 2 Motor Alternators, one to provide a 400Hz supply for the CPU, the other to provide a regulated 50Hz supply for the Plated wire store and the remainder of the configuration. The processor and store impose the following loadings:

CPU + PPU	54KVA	400 Hz
FPU	8KVA	400 Hz
128K	7.5KVA	50 Hz
192K	15KVA	50 Hz
256K	15KVA	50 Hz
384K	22.5KVA	50 Hz
512K	30KVA	50 Hz

6.2.2 The mains supply required is 3 phase 50 Hz with a nominal voltage in the range 220-250/382-433V.

6.3 Environment

Temperature range	$21^{o}C \pm 2^{o}C$ Ambient
Relative Humidity	50% $\pm$ 5% RH
Cleanliness	95% efficiency at particle size down to 1 micron.

The cooling units require a supply of chilled water; for a maximum CPU configuration the requirements are:

91 gals/min at $7^{o}C \pm 2^{o}C$

6.4 Site Layout

CED Environmental Engineering should be consulted regarding all site layout details.

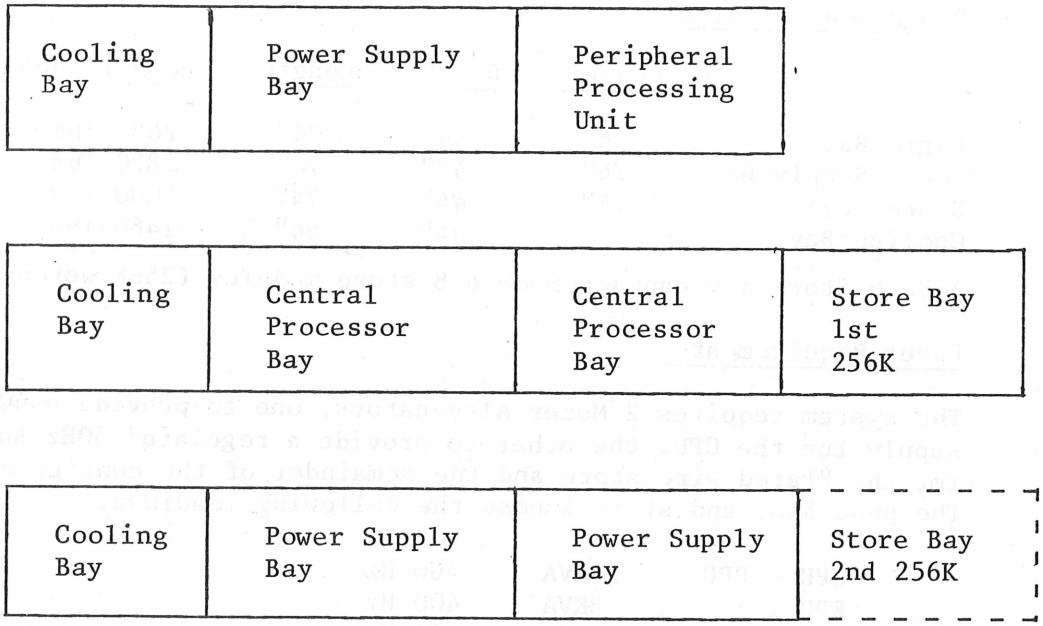

Figure 7 Plan view of bay assemblies

7.0 FIELD ENHANCEMENTS

Because of the small number of 1906S systems field enhancement documentation is produced only when an enhancement is ordered. For details of the work involved in fitting any enhancement, estimated system down-time, testing time, etc. consult CED.

8.0 PERFORMANCE

8.1 Introduction

8.1.1 The 1906S is an asynchronous system in which up to 8 instructions can be overlapped. Individual instruction times can therefore vary widely from the average and cease to have any real significance. The execution time for any given instruction depends on:

a) the sequence of instructions preceding and following,

b) the degree of store interleaving,

c) the location of operands and instructions in main store affecting the number of store clashes,

d) X - register clashes - delays caused when an instruction requires access to an accumulator that is still being used by a previous instruction.

For branch instruction the timing also depends on the availability of the condition to be tested.

The figures quoted include allowance for store clashes and, for branch instructions, are dependent on the condition to be tested being immediately available. No allowance is made for X - register clashes. The effect of these is strongly dependent on the detailed coding of a particular program and could cause variations of up to 20%.

8.1.2 A more meaningful indication of the central processor speed is given by the time taken to perform various instruction loops or sequences; some such times are quoted for specified loops.

8.1.3 Performance may be degraded due to peripheral transfers; for details see page 620.9 para 5.3.5. The processor performance will also be degraded by about 8% if the main store exceeds 256K words.

8.2 Work Mix Times & Loop Times

The following timings are applicable to a system having a 4-way interleaved store not exceeding 256K words.

POWU II	0.65 milliseconds
Loop 1	2.58 microseconds
Loop 2	3.23 microseconds
Loop 3	2.37 microseconds

GAMM Mix (with H/W option F1148/00)

a)	Normal precision, Compact Mode	2.4	Microseconds
b)	Normal precision, Extended Mode	TBA	
c)	Extended precision, Compact Mode	3.6	Microseconds
d)	Extended precision, Extended Mode	TBA	

Loop 4	Scalar Product	4.25	Microseconds
Loop 5	Polynomial (Compact Store, Single precision)	1.72	Microseconds
Loop 6	Polynomial (Extended store, Single precision)	2.03	Microseconds
Loop 7	Polynomial (Compact store, Double precision)	2.46	Microseconds
Loop 8	Polynomial (Extended store, Double precision)	2.73	Microseconds
Loop 9	Line by line compare of tables (Compact store)	3.68	Microseconds
Loop 10	Line by line compare of tables (Extended store)	3.64	Microseconds

Loops 1-10 are defined as follows:-

```
Loop 1   000 5 1/A
         011 5 2/B
         101 1 3/1
         001 2  3
         001 6 3/C
         060 3 S+5

Loop 2   001 7 5
         000 5 1/A
         041 5 2/B
         101 1  1
         101 2  1
         066 4 S-5

Loop 3   000 7 1/A
         101 1  1
         011 7 2/B
         101 2  1
         066 4 S-4

Loop 4   137 0 8N
         137 2 8N+2
         136 0 1/8A
         134 1 2/8B+2
         132 2 8N
         101 1 4
         101 2 4
         066 4 S-7

Loop 5   132 0 1/TABLE
         134 0 CONS
         062 1 S-2
```

First instruction assumed to be in location 8M where N and M are any number.

```
Loop 6      132     0     TABLE
            134     0     CONS
            101    1/2
            066     4     S-3

Loop 7      132     2     1/TABLE
            134     2     CONS
            062     1     S-2

Loop 8      132     2     1/TABLE
            134     2     CONS
            101    1/2
            066     4     S-3

Loop 9      136     0     2/TABLE
            133    0/4
            076     1/DIFF
            062     2     S-3

Loop 10     136     0     3/TABLE
            133    0/4
            076     1/DIFF
            101    3/2
            066     2     S-4
```

8.3 Basic Function Code & Timings

The timings quoted below apply to a 4-way interleaved store and are based on the average time to perform an instruction when it is repeated a large number of times. In some cases this is equal to the function execution time, i.e. time in arithmetic unit or other logic unit, since all instruction fetching and preparation time is lost in the overlap.

All branch instructions are dependent on the conditions to be tested being immediately available.

Function Number	Function Name	Timing in microseconds
000	LDX	0.34
001	ADX	0.34
002	NGX	0.34
003	SBX	0.34
004	LDXC	0.34
005	ADXC	0.34
006	NGXC	0.34
007	SBXC	0.34
010	STO	0.52
011	ADS	0.64
012	NGS	0.52
013	SBS	0.64
014	STOC	0.52
015	ADSC	0.64
016	NGSC	0.52
017	SBSC	0.64
020	ANDX	0.34
021	ORX	0.34
022	ERX	0.34
023	OBEY	0.84
024	LDCH	0.34
025	LDEX	0.34
026	TXU	0.34
027	TXL	0.34
030	ANDS	0.64
031	ORS	0.64
032	ERS	0.64
033	STOZ	0.52
034	DCH	0.64
035	DEX	0.64
036	DSA	0.64
037	DLA	0.64
040	MPY	1.33
041	MPR	1.33
042	MPA	1.33
043	CDB	0.65
044	DVD	1.77
045	DVR	1.77
046	DVS	1.77
047	CBD	1.03
050	BZE	0.79
052	BNZ	0.79
054	BPZ	0.79
056	BNG	0.79

Function Number	Function Name	Timing in microseconds
060	BUX	0.79
062	BDX	0.79
064	BCHX	0.80
066	BCT	0.79
070	CALL	0.90
072	EXIT	0.73
074	BRN etc.	0.73
076	BFP	0.85
100	LDN	0.28
101	ADN	0.32
102	NGN	0.28
103	SBN	0.32
104	LDNC	0.28
105	ADNC	0.32
106	NGNC	0.28
107	SBNC	0.32
110	SLC (1)	0.56
111	SCL (1)	0.61
112	SRC (1)	0.56
113	SRC (1)	0.61
114	NORM	0.47
115	NORM	0.47
116	MVCH(2)	107.52
117	SMO	0.53
120	ANON	0.32
121	ORN	0.32
122	ERN	0.32
123	NULL	0.28
124	IDCT	0.28
125	MODE	1.22
126	MOVE(3)	44.15
127	SUM (4)	54.34

(1) Timing given is for a shift of 10 places

(2) Timing given is for 100 characters moved

(3) Timing given is for 100 words moved

(4) Timing for 100 words.

8.4 Floating Point Unit Function Code & Timings

The following times are those experienced if the same instruction if repeated a large number of times.

Normal Precision Operation

Function		Timing in microseconds
130	FLOAT	0.68
131	FIX	0.67
132	FAD	0.85
133	FSB	0.85
134	FMPY	1.96
135	FDVD	5.08
136	LFP	0.67
137	SFP	0.67

Extended Precision Operation

Function	Timing in microseconds
132	0.84
133	0.94
134	3.05
135	8.93
136	0.84

9.0 ORDER VETTING CHECKLIST

1. Check that the correct system number has been quoted.
2. Check that peripherals specified are supported by GEORGE 3/4 Executive. See Appendix A.
3. Check peripheral simultaneity and that the correct quantity and types of I/O channels have been specified for the connection of all peripherals. See 3.2 and Appendix B.
4. Where peripheral switches or communications equipment have been specified check that configuration diagrams have been supplied.
5. When peripherals are withdrawn ensure that the configuration still contains those required for maintenance purposes and by the Operating System. See 9.1 below and Section 2.0.

9.1 Mandatory Peripherals Required for Maintenance Purposes

INPUT DEVICE

Either an 80 column card reader or paper tape reader

OUTPUT DEVICE

Line printer with 96 or more print positions.

TABLE 1 1906A & 1906S Locally Connected Peripherals

Peripheral Type Number	Executive	
	EWG3	EWG4
Card Equipment		
1911	C(R)	C(R)
1912	C	C
2101/00,01,02	C	C
2102	C	C
2104	C	C
1920/02	C	C
1922/01	C(R)	C(R)
2151	C	C
Paper Tape Equipment		
1915/02	C	C
1916/02	C	C
1925/02	C	C
Line Printers		
1931	C	C
1932	C	C
1933	C	C
2401	C	C
2402	C	C
2408	C	C
2409	C	C
2430	C	C
Magnetic Tape Systems		
1971	C	C
1972	C	C
1973	C	C
2504	C	C
2505	C	C
2506	C	C
2507	C	C
2508	C	C
2509	C	C
Magnetic Drums		
1964	C(R)	C(R)
2851/01+2851/02	C	C
2851/01+2851/04	C	C
Fixed Disc Stores		
2803/01+2805	C(R)	C(R)
2803/02+2806	C(R)	C(R)

TABLE 1 (Continued)

Peripheral Type Number	Executive	
	EWG3	EWG4
Exchangeable Disc Stores		
2801	C	C
2802	C	C
2812/01, 02	C	C
2812/03	C	C
Graph Plotter		
1934	C	C
Document Readers		
8201	C	P
8301	C	P
8401	C	P
Inter-Processor Buffer		
7210	C	C
Local Videos		
7154+7151	C	C
7180+7181/04	C	C
Comms.		
7070/2)	C	C
7070/3 } Uniplexors	C	X
7070/5)	C	C
7901)	C	C
7903 } Processors	C	C
7905)	C	C

TABLE 2 1906A & 1906S Communications Terminals

Terminal Type	Connected Via	Executive	
		EWG3	EWG4
Local Videos			
7151	7154	C	C
Remote Videos			
7153	7070/3	C	X
	7901	C	C
	7903	C	C
	7905	C	C
7181/02	7901	C	C
	7903	C	C
	7905	C	C
7502	7901	C	C
	7903	C	C
	7905	C	C
7503	7901	C	C
	7903	C	C
	7905	C	C
Batch Terminal			
7020/01-05	7901	C	C
	7903	C	C
	7905	C	C
7503	7901	C	C
	7903	C	C
	7905	C	C
Teletypes			
7071 & 7072	7070/02 & /05	C	C
	7901	C	C
	7903	C	C
	7905	C	C
Termiprinters			
7083-6	7070/05	C	C
	7901	C	C
	7903	C	C
	7905	C	C

APPENDIX B

1906A & 1906S PERIPHERAL SIMULTANEITY RULES

1.0 INTRODUCTION

1.0.1 These rules determine the load that each peripheral puts on the system and the type of Standard Interface required for each peripheral connection. The number of interfaces of each type available and the total peripheral loading permitted on a system are dependent on the processor type: for details see the appropriate processor entry para. 3.2.2. (For 1906A see page 610.5 and for 1906S see page 620.5).

1.0.2 Peripheral loadings are expressed as IMTAC values which for all Fast Peripherals and High Speed Peripherals are the same as those used on 1903T, 1904A and 1904S. IMTAC value means the Inverse Mean Time between Accesses to Core Store and is derived by dividing the minimum period in microseconds between peripheral requests for data transfer into 1000. For example, the 2505 (160 Kch/s Magnetic Tape Control) can request a transfer once every 23 microseconds if all tolerences are additive, hence

$$\frac{1000}{23} = 44 = \text{IMTAC value for 2505.}$$

On 1906A and 1906S the loadings that Slow Peripherals put on the PPU have also been expressed as IMTAC values for convenience although the method of deriving these values is quite different from the above. The IMTAC values assigned to Slow Peripherals are numerically different from the oc- factors used on 1903T, 1904A and 1904S; IMTAC value is approximately equal $\frac{\text{oc- factor}}{2}$

1.0.3 It is emphasised that the inclusion of peripherals in the tables given in the following rules cannot be taken as an authority that these peripherals may be offered for sale with any 1906A or 1906S. See the appropriate Approved Central Processor/ Peripheral Connections tables given in Appendix A.

2.0 HIGH SPEED PERIPHERALS

2.0.1 High Speed Peripherals are those which operate under the F=1 fast standard interface timing rules and must be connected via High Speed Peripheral Standard Interfaces (also called High Speed Channels). Table 1 lists the High Speed Peripherals and the IMTAC value assigned to each. For details of the number of High Speed Peripheral Standard Interfaces available, the sequence of ordering them and the maximum permitted loading per block (or High Speed Control) see the appropriate processor entry para. 3.2.2.

2.0.2 Some peripherals may operate under either F=1, or F=0 timing rules and may therefore be connected to either High Speed Peripheral Standard Interfaces or Fast Peripheral Standard Interfaces; these will be found listed in both Tables 1 and 2.

2.0.3 It is not permitted to mix High Speed Peripherals and Fast Peripherals on the same control. When a block of High Speed Peripheral Standard Interface has been specified for use as a block of Fast Peripheral Standard Interfaces then only Fast Peripherals may be connected to them. Similarly only High Speed Peripherals may be connected to any block of High Speed Peripheral Standard Interfaces specified for normal use in F=1 mode.

TABLE 1 HIGH SPEED PERIPHERAL LOADING

Peripheral	IMTAC Value
2851/01 + 2851/02 High Speed Drum	350
F1216 + 2851/02 High Speed Drum	350
2851/01 + 2851/04 High Speed Drum	88
F1216 + 2851/01 High Speed Drum	88
2803/02 + 2806 Fixed Disc Store	75
F1181 + 2806 Fixed Disc Store	75

3.0 FAST PERIPHERALS

3.0.1 Fast Peripherals are those which transfer data in 4-character bursts (Burst Mode) under F=0 timing rules and must be connected via Fast Peripheral Standard Interfaces (also known as Fast Channels). Table 2 lists the Fast Peripherals and the IMTAC value assigned to each. For details of the number of Fast Peripheral Standard Interfaces available and the sequence of ordering them, see the appropriate processor entry para. 3.2.2.

3.0.2 The total IMTAC value of all peripherals connected to any block of Fast Peripheral Standard Interfaces, or any block of High Speed Standard Interfaces used as Fast Peripheral Standard Interfaces, must not exceed 112.5.

3.0.3 Some types of Fast Peripherals are capable of transferring data at the maximum rate which a Fast Control will allow, although this maximum transfer rate will not be maintained and is not necessary in order to obtain the maximum throughput via the peripheral. Such peripherals have an IMTAC value which can vary between the value required to maintain maximum peripheral throughput, shown in parenthesis in Table 2, and 112.5. If a configuration includes any of these peripherals, then peripherals will be grouped such that the total IMTAC value of all peripherals on any Fast Control (Block of Fast Peripheral Standard Interfaces), having one of these variable IMTAC value peripherals, will be as close to 112.5 as possible without exceeding it. The IMTAC value to be used for this purpose is the one shown in parenthesis in Table 2.

3.0.4 It is possible to re-arrange the peripheral connections to satisfy 3.0.2 and 3.0.3 when additional peripherals are installed in the field.

NOTE. The combination of EDS 30 or EDS 60 and 9-Track MT systems on the same Fast Control should be avoided if possible. When this cannot be achieved within the above rules, the configuration should be referred to Divisional S&TS.

TABLE 2 FAST PERIPHERAL LOADING

Peripheral	IMTAC Value
2851/01 + 2851/04 High Speed Drum	88
F1216/ + 2851/04 High Speed Drum	88
1964 512K word Drum	29
1963 128K word Drum	29
1962 32K word Drum	13.6
9372/1 Burroughs Fixed Head Disc	77
2803/01 + 2805 FDS	49
F1083 + 2805 FDS	49
2803/02 + 2806 FDS	75
F1181 + 2806 FDS	75
2801/00 4M EDS	55.5
2802/00 8M EDS	55.5
2812/01 EDS 30	(56) Max 112.5
2812/02 EDS 30	(56) Max 112.5
2812/03 EDS 60	(56) Max 112.5
1972 40Kch/s NRZ 7T MT	13
1973 60Kch/s NRZ 7T MT	19
2504 80Kch/s PE 9T MT	22
2505 160Kch/s PE 9T MT	44
2506 40Kch/s NRZ 9T MT	11
2507 80Kch/s NRZ 9T MT	22
2508 80Kch/s PE 9T MT	22
2509 160Kch/s PE 9T MT	44
1931 300 lpm Line Printer	(12.8) Max 112.5
1932 600 lpm Line Printer	(25.7) Max 112.5
2401 300 lpm Line Printer	(14.4) Max 112.5
2402 600 lpm Line Printer	(20.0) Max 112.5
7154/01 Visual Display Unit 520 ch.	10.4
7154/02 Visual Display Unit 1040 ch.	20.8
7180/02 Video Cluster Controller	50.0
7901 Communications Processor	(1) Max 45.0
7903 Communications Processor	(8) Max 112.5
7905 Communications Processor	(10) Max 112.5
7203/03 BSI to 1900 SI Converter (See note 1)	(X) Max 112.5
7210/01 Inter-Processor Buffer (See note 2)	(Y) Max 59
8500 Document Sorter/Reader	2.6

Notes: 1. X = Transfer rate required in $\frac{\text{Kch./sec}}{4}$

2. $Y = \frac{112.5S}{450.+S}$ Where S = Transfer rate of the Standard Interface on the other Processor.

4.0 SLOW PERIPHERALS

4.0.1 Table 3 lists the slow peripherals (i.e. single-character peripherals) and the IMTAC value assigned to each.

4.0.2 The total IMTAC value for all peripherals connected via Slow Peripheral Standard Interfaces is the sum of the individual peripheral IMTAC values and must not exceed 200.

4.0.3 An IMTAC value of zero can be taken for all non-crisistime peripherals which will occupy the lowest priority sockets on the Slow Control but maximum throughput via these peripherals cannot then be guaranteed. If the maximum throughput is important then the values given in parenthesis in Table 3 should be used for all such peripherals.

5.0 MAXIMUM SYSTEM LOADING

The total IMTAC value for the system is defined below and is dependent on the processor type; see appropriate processor entry para. 3.2.2 for the maximum value permitted.

Total IMTAC value per system is the sum of the IMTAC values of all peripherals connected to High Speed and Slow Standard Interfaces plus the "Apparent IMTAC value" of all peripherals connected to Fast Peripheral Standard Interfaces.

The "Apparent IMTAC value" for the Fast Peripherals is defined as follows:-

a) If the Fast Peripheral Standard Interfaces do not have any of the variable IMTAC value peripherals (see 3.0.3) then the "Apparent IMTAC value" is the sum of the individual peripherals actual IMTAC values as specified in Table 2.

b) If any one or several of the Fast Peripheral Standard Interface Blocks have any of the variable IMTAC value peripherals connected then the "Apparent IMTAC value" for all peripheral connected via the Fast Peripheral Standard Interfaces equals 112.5 for each of the blocks which have such peripherals plus the sum of the IMTAC values of peripherals connected to any other blocks.

TABLE 3 SLOW PERIPHERAL LOADING

Peripheral	IMTAC Value
1971 20Kch/s NRZ 7T MT	103
1911 900 cpm 80 col. Card Reader	9.3
1911 + F911 (Card Image)	18.5
1912 300 cpm 80 col. Card Reader	6.6
1912 + F912 (Card Image)	13.2
2101/00 1200 cpm 80 col. Card Reader	12.7
2101/00 + F1154 (Card Image)	25.4
2101/01 1600 cpm 80 col. Card Reader	19.1
2101/01 + F1154 (Card Image)	38.2
2101/02 2000 cpm 80 col. Card Reader	21.7
2101/02 + F1154 (Card Image)	43.4
2102 300 cpm 80 col. Card Reader	6.2
2103 600 cpm 40 col. Card Reader	12.5
2104 600 cpm 80 col. Card Reader	13.7
2104 + F1155 (Card Image)	27.4
1920 100 cpm 80 col. Card Punch	12.8
1922 33 cpm 80 col. Card Punch (see note 1)	0 (0.2)
2151 300 cpm 80 col. Card Punch	8.3
1915/02 300 cps Paper Tape Reader } See note 1	0 (1.2)
1916/02 1000 cps Paper Tape Reader } See note 1	0 (4.0)
1925/02 110 cps Paper Tape Punch } See note 1	0 (0.5)
1933 1350 lpm Line Printer } see note 1	0 (14.4)
2408 300 lpm Line Printer } see note 1	0 (3.0)
2409 600 lpm Line Printer } see note 1	0 (6.0)
2430 High Speed Train Printer } see note 1	0 (15.0)
1934 Graph Plotter (see note 1)	0 (1.3)
8201/01 Optical Character Reader	2.5
8301/01 Optical Mark Reader	32.4
8401/01 Optical Character/Mark Reader (See note 2)	34.9
7010/03 Telephone Data Terminal 600/1200 bps	0.6
7010/05 Telephone Data Terminal 2400 bps	1.2
7010/07 Telephone Data Terminal 4800 bps	2.4
7070 + 7071 Interrogating Typewriter	0.5
7070/01 Telegraph Data Terminal 5 bit	0.3
7070/02 Telegraph Data Terminal 8 bit	0.4
7070/03 Telephone Data Terminal Remote VDU	0.6
7070/05 Telephone Data Terminal 8 bit	0.5
7203/01, /02 BSI to 1900 SI Converter Sch+ISO (see note 1)	0 (100)

Notes: 1. Peripherals with no crisistime, but an IMTAC value for maximum throughput is given in parenthesis.

2. Requires 2 Slow Peripheral Standard Interfaces.

6.0 EXAMPLE OF USE OF THE SIMULTANEITY RULES

Consider the following configuration:

2082/00 Processor + 2080/04 256K words Store

2 x 2851/01 + 2 x 2851/02
4 x 2812/03 + 4 x 2816/02
2 x 2802/00 + 4 x 2802/02
4 x 2509/02
1 x 1972/02
2 x 2101/00
1 x F1154
1 x 1920/02
2 x 1916/02
2 x 1925/02
1 x 1934
4 x 1933/03
1 x 7903/00 + 7903/02 + Communications configuration.

The method of checking this configuration is set out opposite.

Note: a) All peripherals listed are supported by Executive; see appendix A.

b) For the purpose of working out the optional interfaces required and checking the peripheral simulataneity it is necessary only to consider the peripheral control units.

c) The IMTAC values given in parenthesis are those required to maintain maximum throughput via variable IMTAC value peripherals. The block loading for any block with such a peripheral automatically becomes the apparent value of 112.5.

d) The peripherals marked thus * are non crisistime peripherals.

e) Priority of servicing the peripherals has not been taken into account and none is implied in the order in which the peripherals or the Blocks of Fast Peripheral Standard Interfaces have been set out.

In this case IMTAC values have been assigned to the non-crisistime peripherals which guarantee maximum throughput via these peripherals and neither the maximum IMTAC value permitted on the Slow Control or the total IMTAC value for the system have been exceeded. Now consider adding one 1971/02 MT Cluster to the system. The configuration will still be valid although maximum throughput via the non-crisistime peripherals cannot be guaranteed.

Peripheral Grouping	I-Face Options Required	IMTAC Values Per Peripheral	Per Block	Max. IMTAC value permitted per Blk.
HIGH SPEED				
2851/01	F1441/00	350	700 ✓	750
2851/01		350		
FAST				
2509/02	Basic 4 Fast	44	112.5 ✓	112.5
2509/02		44		
1972/02		13		
7903/00		(8.0)		
2812/03	F1397/00	(56)	112.5 ✓	112.5
2812/03		(56)		
2812/03	F1437/00	(56)	112.5 ✓	112.5
2812/03		(56)		
2802/00	F1438/00	55.5	99.5 ✓	112.5
2509/02		44		
2802/00	F1439/00	55.5	99.5 ✓	112.5
2509/02		44		
SLOW				
2101/00+F1154	Basic 10 Slow	25.4	118.8 ✓	200
2101/00		12.7		
1920/02		12.8		
1916/02		4.0*		
1916/02		4.0*		
1925/02		0.5*		
1925/02		0.5*		
1934		1.3*		
1933/03		14.4*		
1933/03		14.4*		
1933/03	F1184/00	14.4*		
1933/03		14.4*		
–				
–				
–				
–				
	TOTAL =		1355.3 ✓	
	MAX. PERMITTED ON 2082 =		1625	

STANDARD INTERFACE SWITCHING ON 1906A & 1906S

Standard Interface switching applications on these systems normally involve the switching of peripherals between two processor systems because on the 1906A or 1906S Systems enough interfaces are available for each peripheral. Under these circumstances there are no special restrictions other than those imposed by the requirements to provide the correct types of Standard Interface connections and to observe the Peripheral Simultaneity Rules given in Appendix B.

The interfacing requirements on the other system may in some circumstances determine the type of interface required on the 1906A or 1906S. For example, where peripherals may be connected to either High Speed Peripheral Standard Interfaces or Fast Peripheral Standard Interfaces the same Standard Interface timing rules (F=0 or F=1) should be used on each system.

Details of Standard Interface Switching Units are given in Section 4.