APPROVED CENTRAL PROCESSOR/PERIPHERAL CONNECTIONS

Processors	1903T 1904A 1904S (including Reduced Facility versions)
Table 1	Locally Connected Peripherals
Table 2	Communications Terminals

Legend

C	=	Connection permitted, Executive module available.
C(R)	=	Connection permitted only if customer is retaining the peripheral from an earlier system. Executive module written.
P	=	Permissible connection but Executive module has not been written. Application must be made to Divisional S. & T.S. Hardware Support Branch to ascertain possible delivery prior to entering into any contractual commitment.
X	=	Connection not permitted.

NOTE: The availability of an Executive or DCP to support a peripheral connection does not imply availability of the peripheral. For hardware availability consult Sales Liaison Dept., ICL House, Putney, S.W.15.

TABLE 1 LOCALLY CONNECTED PERIPHERALS

Peripheral Type Number	Non-Paged			Paged
	1904A	1903T, 1904A, 1904S		
	E6BM	E6RM	EWG3	EWG4
Card Equipment				
1911	C	C	C	C
1912	C	C	C	C
2101/00,01,02	C	C	C	C
2102	C	C	C	C
2103	C(R)	C(R)	C(R)	X
2104	C	C	C	C
1920/02	C	C	C	C
1922/01	C(R)	C(R)	C(R)	C(R)
2151	C	C	C	C
Paper Tape Equipment				
1915/02	C	C	C	C
1916/02	C	C	C	C
1925/02	C	C	C	C
2601/01	X	C(R)	C(R)	C(R)
2602/01	X	C(R)	C(R)	C(R)
Line Printers				
1931	C	C	C	C
1932	C	C	C	C
1933	C	C	C	C
2401	C	C	C	C
2402	C	C	C	C
2408	X	C	C	C
2409	X	C	C	C
2430	X	C	C	C
Magnetic Tape Systems				
1971	C	C	C	C
1972	C	C	C	C
1973	C	C	C	C
2504	C	C	C	C
2505	C	C	C	C
2506	C	C	C	C
2507	C	C	C	C
2508	C	C	C	C
2509	C	C	C	C
Magnetic Drums				
1964	C(R)	C(R)	C(R)	C(R)
2851/01+2851/02	X	X	C	C
2851/01+2851/04	X	X	C	C
Fixed Disc Stores				
2803/01+2805	C(R)	C(R)	C(R)	C(R)
2803/02+2806	C(R)	C(R)	C(R)	C(R)

TABLE 1 (Continued)

Peripheral Type Number	Non-Paged			Paged
	1904A	1903T, 1904A, 1904S		
	E6BM	E6RM	EWG3	EWG4
Exchangeable Disc Stores				
2801	C(R)	C	C	C
2802	C(R)	C	C	C
2812/01,02	X	C	C	C
2812/03	X	C	C	C
Graph Plotter				
1934	C	C	C	C
Document Readers				
8201	C	C	C	P
8301	C	C	C	P
8401	C	C	C	P
Inter-Processor Buffer				
7210	C	C	C	C
Local Videos				
7154+7151	C	C	C	C
7180+7181/04	C	C	C	C
Comms.				
7007 Multiplexor	C(R)	C(R)	C(R)	X
7010/1-7) Uniplexors	C	C	C	C
7070/2) Uniplexors	C	C	C	C
7070/3) Uniplexors	C	C	C	X
7070/5) Uniplexors	C	C	C	C
7901) Processors	C	C	C	C
7903) Processors	C	C	C	C
7905) Processors	X	C	C	C
7920) Scanners	C	C	C	X
7930) Scanners	C	C	C	X

TABLE 2 COMMUNICATIONS TERMINALS

Terminal Type	Connected Via	Non-Paged			Paged
		1904A	1903T, 1904A, 1904S		
		E6BM	E6RM	EWG3	EWG4
Local Videos					
7151	7154	C	C	C	C
Remote Videos					
7153	7070/3	C	C	C	C
	7920	X	X	X	X
	7930	X	X	X	X
	7901	C	C	C	C
	7903	C	C	C	C
	7905	X	C	C	C
7181/02	7920	C	C	C	X
	7930	C	C	C	X
	7901	C	C	C	C
	7903	C	C	C	C
	7905	X	C	C	C
7502	7920	C	C	C	X
	7930	C	C	C	X
	7901	C	C	C	C
	7903	C	C	C	C
	7905	X	C	C	C
7503	7920	C	C	C	X
	7930	C	C	C	X
	7901	C	C	C	X
	7903	C	C	C	C
	7905	X	C	C	C
Batch Terminal					
7020/01-05	7007	C	C	C	X
	7010/01-07	C	C	C	C
	7920	C	C	C	X
	7930	C	C	C	X
	7901	C	C	C	C
	7903	C	C	C	C
	7905	X	C	C	C
7503	7007	X	X	X	X
	7010/01-07	X	X	X	X
	7920	C	C	C	X
	7930	C	C	C	X
	7901	C	C	C	C
	7903	C	C	C	C
	7905	X	C	C	C
Teletypes					
7071&7072	7007	C	C	C	X
	7070/02&/05	C	C	C	C
	7920	C	C	C	X

TABLE 2 (Continued)

Terminal Type	Connected Via	Non-Paged			Paged
		1904A	1903T, 1904A, 1904S		
		E6BM	E6RM	EWG3	EWG4
Teletypes (Cont'd)					
	7930	C	C	C	C
	7901	C	C	C	C
	7903	C	C	C	C
	7905	X	C	C	C
Termiprinters					
7083-6	7070/05	C	C	C	C
	7920	C	C	C	X
	7930	C	C	C	X
	7901	C	C	C	C
	7903	C	C	C	C
	7905	X	C	C	C

1903T, 1904A, 1904S Peripheral Simultaneity Rules

1.0 INTRODUCTION

1.0.1 All peripherals connected to a 1903T, 1904A or 1904S system must be able to run simultaneously and the correct I/O channels must be provided for their connection. The rules given below determine the type of channel required for each peripheral connection and the loading that each peripheral puts on the system. The number of channels of each type available and the total peripheral loading permitted on a system are dependent on the processor type; see appropriate processor entry par. 3.1. (For 1903T see page 510.3, for 1904A see page 520.3, for Interim 1904S see page 530.3 and for 1904S see page 540.3).

1.0.2 The PAC and the SHC loadings must be calculated separately. Two values are given for the permitted loading on the PAC for each processor type depending on whether or not any High Speed Channels are used. The loading permitted on the SHC is dependent on both the processor type and the actual loading on the PAC in each case and is derived by a simple formulae. One formulae is given for each processor type.

1.0.3 Two terms are used to express peripheral loading:

a) IMTAC value, meaning the Inverse Mean Time between Accesses to Core store (or semiconductor store) and is derived by dividing the minimum period in microseconds between peripheral requests for data transfer into 1000. For example, the 2505 (160 Kch/s Magnetic Tape Control) can request a transfer once every 23 microseconds if all tolerences are additive, hence

$$\frac{1000}{23} = 44 = \text{IMTAC value for 2505.}$$

On 1903T, 1904A and 1904S systems IMTAC values apply only to burst-mode peripherals that are connected to a PAC via either High Speed or Fast channels. The IMTAC values that are assigned to such peripherals are the same as are used on 1906A and 1906S systems.

b) $\propto$ Factor. This is a measure of how heavily a peripheral loads the SHC of the processor to which it is connected. Each peripheral, which may be connected to the SHC, is given an $\propto$ factor. Peripherals which may be connected to either the PAC or the SHC will have both an IMTAC value and an $\propto$ factor and these are numerically different.

1.0.4 It is emphasised that the inclusion of peripherals in the tables given in the following rules cannot be taken as an authority that these peripherals can be offered for sale with any 1903T, 1904A or 1904S processor. See Appendix A,

Approved Central Processor/Peripheral Connections table for the particular processor and the type of Executive to be used with it.

2.0 HIGH SPEED CHANNEL

2.0.1 A High Speed Channel F1162/00) operates in F=1 mode, that is under Standard Interface fast timing rules, and allows for the connection of higher data transfer rate peripherals than could otherwise be handled on PAC through the normal Fast Channels. Table 1 lists the peripherals that may be connected via High Speed Channels and the IMTAC value assigned to each peripheral. The number of High Speed Channels available on a particular processor are dependant on the processor type, see appropriate processor entry par. 3.1.

TABLE 1 HIGH SPEED CHANNELS

Peripheral	IMTAC Value
2851/01 + 2851/02 High Speed Drum	350
F1216 + 2851/02 High Speed Drum	350
2851/01 + 2851/04 High Speed Drum	88
F1216 + 2851/04 High Speed Drum	88
2803/02 + 2806 Fixed Disc Store	75
F1181 + 2806 Fixed Disc Store	75
Maximum IMTAC value allowed on a High Speed Channel	375

2.0.2 Some peripherals may be connected either via High Speed or Fast Channels and will be listed in both Tables 1 and 2. The choice of connection is left to the customer and may be determined by the fact that if such a peripheral is to be shared by some other processor via a Standard Interface Switching Unit, then the interfacing on the other processor may determine whether F=0 (Fast Channel) or F=1 (High Speed Channel) rules apply. It makes no difference to Executive or to hesitation time whichever method of connection is used, but it is essential that all orders clearly specify whether a peripheral listed in both tables is to be connected via a Fast Channel or via a High Speed Channel.

2.0.3 On 1903T, 1904A or 1904S processors the High Speed Channels may not be used as Fast Channels.

3.0 FAST CHANNELS

3.0.1 Fast Channels (F1161/00) operate in F=0 mode, that is under the normal Standard Interface timing rules. They are connected to fast data buffers in a PAC; each data buffer may have one or several Fast Channels connected to it but no Fast Channel may be connected to more than one data buffer. Data buffers are supplied as required up to the maximum number available depending on the processor type, see appropriate processor entry par. 3.1. The peripherals which may be connected via Fast Channels and the IMTAC value assigned to each are listed in Table 2.

3.0.2 The total IMTAC value of all peripherals connected to any one data buffer must not exceed 95. This introduces a restriction on the number and type of peripherals attachable via Fast Channels such that neither the number of data buffers available or the maximum IMTAC value allowed on any data buffer is exceeded.

3.0.3 Some types of peripherals are capable of transferring data at the maximum rate which a data buffer will allow, although this maximum transfer rate will not be maintained and is not necessary in order to obtain the maximum throughput via the peripheral. Such peripherals have an IMTAC value which can vary between the value required to maintain maximum peripheral throughput, shown in parenthesis in Table 2, and 95. If a configuration includes any of these peripherals, then peripherals will be grouped such that the total IMTAC value of all peripherals on any data buffer, having one of these variable IMTAC value peripherals, will be as close to 95 as possible without exceeding it. The IMTAC value to be used for this purpose is the one shown in parenthesis in Table 2.

3.0.4 Normally any one of the variable IMTAC value peripherals will be connected to the lowest priority socket of a data buffer. The only exception to this rule is if 2 or more unbuffered line printers are attached to one data buffer, then they will occupy the lowest priority sockets on that data buffer.

3.0.5 It is possible to rearrange the interconnections between Fast Channels and data buffers to achieve the conditions stated in 3.0.3 and 3.0.4 when additional peripherals are installed in the field.

3.0.6 The total IMTAC value on a PAC is the sum of the IMTAC value of any peripheral connected to the High Speed Channel and the "Apparent IMTAC value" of the peripherals connected via the Fast Channels on that PAC where "Apparent IMTAC value" is defined as follows:

TABLE 2 FAST CHANNELS

Peripheral	IMTAC Value
2851/01 + 2851/04 High Speed Drum	88
F1216 + 2851/04 High Speed Drum	88
1964 512K word Drum	29
1963 128K word Drum	29
1962 32K word Drum	13.6
9372/1 Burroughs Fixed Head Disc	77
2803/01 + 2805 FDS	49
F1083 + 2805 FDS	49
2803/02 + 2806 FDS	75
F1181 + 2806 FDS	75
2801/00 4M EDS	55.5
2802/00 8M EDS	55.5
2812/01 EDS 30	(56) Max.95
2812/02 EDS 30	(56) Max.95
2812/03 EDS 30	(56) Max.95
1972 40Kch/s NRZ 7T MT	13
1973 60Kch/s NRZ 7T MT	19
2504 80Kch/s PE 9T MT	22
2505 160Kch/s PE 9T MT	44
2506 40Kch/s NRZ 9T MT	11
2507 80Kch/s NRZ 9T MT	22
2508 80Kch/s PE 9T MT	22
2509 160Kch/s PE 9T MT	44
1931 300 lpm Line Printer) (See	(12.8)Max.95
1932 600 lpm Line Printer) note	(25.7)Max.95
2401 300 lpm Line Printer (see note 1)) 5)	(14.4)Max.95
2402 600 lpm Line Printer)	(20.0)Max.95
7154/01 Visual Display Unit 520ch.	10.4
7154/02 Visual Display Unit 1040ch.	20.8
7180/02 Video Cluster Controller	50.0
7903 Communications Processor	(8.0) Max.95
7905 Communications Processor	(10.0) Max.95
7203/03 BSI to 1900 SI Converter (see note 2)	(X) Max.95
7210 Inter-Processor Buffer (see note 3)	Y
8500 Document Sorter/Reader (see note 4)	2.6

Notes: 1. Modification No. 190/L/5004 is necessary on any 2401 Line Printer to be connected to PAC via a Fast Channel.

2. X = Transfer rate required in $\frac{\text{Kch/sec.}}{4}$

3. $Y = \frac{95S}{380+S}$ where S = Transfer rate of the Standard Interface on the other processor.

4. Refer to your S.&T.S. Divisional Technical Support Branch if the number of 8500's to be connected exceeds 2.

5. Refer to your S.&T.S. Divisional Technical Support Branch if any unbuffered Line Printer and an EDS 4M or 8M are required to share the same data buffer on PAC.

a) If the Fast Channels do not have any of the variable IMTAC value peripherals connected to them, then the "Apparent IMTAC value" is the sum of the individual peripherals actual IMTAC values as given in Table 2.

b) If any data buffer associated with Fast Channels has one or more of the variable IMTAC value peripherals then the "Apparent IMTAC value" for all peripherals connected to that data buffer is equal to 95. The total "Apparent IMTAC value" for all peripherals connected via Fast Channels on that PAC is the sum of the "Apparent IMTAC values", that is 95 for each data buffer which has any variable IMTAC value peripheral plus the IMTAC values of all peripherals connected to other data buffers which do not have such peripherals.

3.0.7 The total IMTAC value for a processor, termed I, is the same as that for PAC, if only one PAC is fitted. If two PACs are fitted, I is equal to the sum of the total IMTAC values for the two PACs. The value of I must not exceed that permitted on any processor, see appropriate processor entry par. 3.1.

4.0 SLOW CHANNELS

4.0.1 Slow Channels (F1163/00) come in groups of six. They operate in F=0 mode and can handle either single character or burst-mode (4-character) peripherals but not more than 6 sockets can be designated for use with multichannel or dual channel peripherals. In all cases one group of 6 Slow Channels is provided with the 1903T, 1904A or 1904S Central Processor and up to two additional groups of 6 can be ordered by specifying F1163/00. Table 3 lists the peripherals which may be connected via Slow Channels and the α factor assigned to each.

4.0.2 The total α factor for all peripherals connected via Slow Channels is the sum of the individual peripherals α factors. The total α factor allowed depends on the processor type and on the total IMTAC value (I) for that processor, see appropriate processor entry par. 3.1.

4.0.3 An α factor of zero can be taken for all non-crisistime peripherals which will occupy the lowest priority sockets on the SHC but maximum throughput via these peripherals cannot then be guaranteed. If the maximum throughput is important then the values given in parenthesis in Table 3 should be used for all such peripherals.

TABLE 3 SLOW CHANNELS

Peripheral	Factor
1962 32K word Drum (see Note 1)	192
1971 20Kch/s NRZ 7T MT (see Note 2)	220
1972 40Kch/s NRZ 7T MT	187
1973 60Kch/s NRZ 7T MT	280
1198/99 1100 MT Converter	182
1911 900 cpm 80 col. Card Reader	18.5
1911 + F911 (Card Image)	37.3
1912 300 cpm 80 col. Card Reader	13.2
1912 + F912 (Card Image)	26.6
2101/00 1200 cpm 80 col. Card Reader	25.4
2101/00 + F1154 (Card Image)	50.8
2101/01 1600 cpm 80 col. Card Reader	38.2
2101/01 + F1154 (Card Image)	77.5
2101/02 2000cpm 80 col. Card Reader	43.4
2101/02 + F1154 (Card Image)	86.8
2102 300 cpm 80 col. Card Reader	12.4
2103 600 cpm 40 col. Card Reader	25.0
2104 600 cpm 80 col. Card Reader	27.4
2104 + F1155 (Card Image)	55.2
1920 100 cpm 80 col. Card Punch	25.6
1922 33 cpm 80 col. Card Punch	0 - (0.4)
2151 300 cpm 80 col. Card Punch	18.7
1915/02 300 cps Paper Tape Reader	0 - (2.4)
1916/02 1000 cps Paper Tape Reader	0 - (7.9)
1916/03 800 cps Paper Tape Reader (Olivetti)	0 - (6.4)
1925/02 110 cps Paper Tape Punch	0 - (0.9)
2601/01 300/110 cps Paper Tape Reader/Punch	0 - (3.3)
2602/0 1000/110 cps Paper Tape Reader/Punch	0 - (8.8)
1931 300 lpm Line Printer (see Note 3)	180
1933 1350 lpm Line Printer	0 - (28.8)
2401 300 lpm Line Printer (see Note 3)	203
2408 300 lpm Line Printer	0 - (6.0)
2409 600 lpm Line Printer	0 - (12.0)
2430 High Speed Train Printer	0 - (30.0)
1934 Graph Plotter	0 - (2.5)
8201/01 Optical Character Reader	5.0
8301/01 Optical Mark Reader	64.8
8401/01 Optical Character/Mark Reader(see note4)	69.8
8500 Document Sorter/Reader (see note 5)	37.2
7010/03 Telephone Data Terminal 600/1200 bps	1.2
7010/05 Telephone Data Terminal 2400 bps	2.4
7010/07 Telephone Data Terminal 4800 bps	4.8
7070 + 7071 Interrogating Typewriter	0.9
7070/01 Telegraph Data Terminal 5 bit	0.6
7070/02 Telegraph Data Terminal 8 bit	0.8
7070/03 Telephone Data Terminal Remote VDU	1.2
7070/05 Telephone Data Terminal 8 bit	0.9
7154/01,/02 Visual Display Unit 520ch./1040ch.	0 - (180)
7180/02 Video Cluster Controller	0 - (500)

TABLE 3 SLOW CHANNELS (continued)

Peripheral	Factor
7007/02 Communications Multiplexor)See 7921/01 + 7920 Scanner Selector + Scanner(s))note 7930/09 + 7930 Scanner Selector + Scanner(s))6	x + y x + y x + y
7901 Communications Processor 7903 Communications Processor 7905 Communications Processor	0 - (10) 0 - (60) 0 - ( )
7203/1, /2 BSI to 1900 SI Converter Sch + ISO 7203/3 BSI to 1900 SI Converter 4-ch 7210 Inter Processor Buffer (see note 7)	0 - (200) 0 - (600) 0 - (X)

Notes:

1. If any drum(s) is connected via a Fast Channel(s), then none may be connected via Slow Channels on the same system.

2. The maximum block length that may be used with 1971 is 8K words.

3. Not more than one 1931 or two 2401's may be connected via Slow Channels on the same system.

4. Each 8401/01 requires two Slow Channels.

5. Refer to your S.&T.S. Divisional Technical Support Branch if the number of 8500's to be connected exceeds 2.

6. $x = B.10^{-3}$ where B = total baudrate of all telephone lines.
   $y = 8B.10^{-3}$ where B = total baudrate of all telegraph lines.

7. $X = \frac{1287S}{286+S}$ where S = Transfer rate of the Standard Interface on the other processor.

Example 2 1904A Configuration

Consider the following peripheral configuration on a 1904A:

1 x 2851/01 — on a High Speed Channel

2 x 2802/00
1 x 2803/02
3 x 1973
1 x 2402
— on Fast Channels

1 x 2101/01 + F1154
1 x 1920
2 x 1933
2 x 1916
1 x 1925
— on Slow Channels

Grouping on PAC data buffers Peripheral	IMTAC-Value		Peripheral on SHC	Factor
2803/02	75	75	2101/01+F1154	77.5
2802	55.5)		1920	25.6
1973	19)	93.5	1933	0 (28.8)
1973	19)		1933	0 (28.8)
2802	55.5)		1916	0 (7.9)
1973	19)	95	1916	0 (7.9)
2402	(20))		1925	0 (0.9)
TOTAL IMTAC-Value = 263.5 on Fast Channels			TOTAL α Factor 103.1 (74.3)	
IMTAC-Value on H/S Channel for 2851/01 = 350			TOTAL α Factor for maximum throughput via the non-crisistime peripherals	
TOTAL IMTAC-Value on PAC(I) = 613.5			= 103.1 + 74.3 = 177.4	

Maximum IMTAC-Value permitted on PAC = 750*
Maximum IMTAC-Value permitted on Fast Channels = 750-350 = 400*
Maximum number of fast data buffer = 6

$\therefore$ the configuration on PAC is valid ($613.5 < 750$ $263.5 < 400$ and ≤ 6 data buffers have been used)

α Factor permitted on SHC = $650 - 0.25I$
$= 650 - 0.25 \times 613.5 = 496.6$

$\therefore$ the configuration on SHC is valid ($177.4 < 496.6$)

*See 3.1.1 page 520.3

The following I/O channels are required:

1 x F1162/00
3 x F1161/00
1 x F1163/00

STANDARD INTERFACE SWITCHING ON 1903T, 1904A & 1904S

Standard Interface switching applications on these systems normally involve the switching of peripherals between two processors because on the 1903T, 1904A or 1904S systems enough interfaces are available for each peripheral. Under these circumstances there are no special restrictions other than those imposed by the requirements to provide the correct types of Standard Interface connections and to observe the Peripheral Simultaneity Rules given in Appendix B.

The interfacing requirements on the other system may in some circumstances determine the type of interface required on the 1903T, 1904A or 1904S. For example, where peripherals may be connected to either High Speed Channels or Fast Channels the same Standard Interface timing rules (F=0 or F=1) should be used on each system.

Details of Standard Interface Switching Units are given in Section 4.